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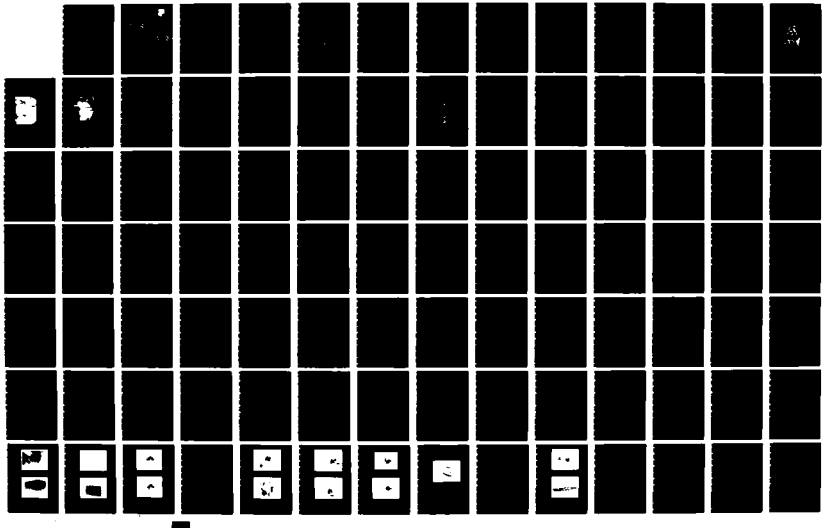

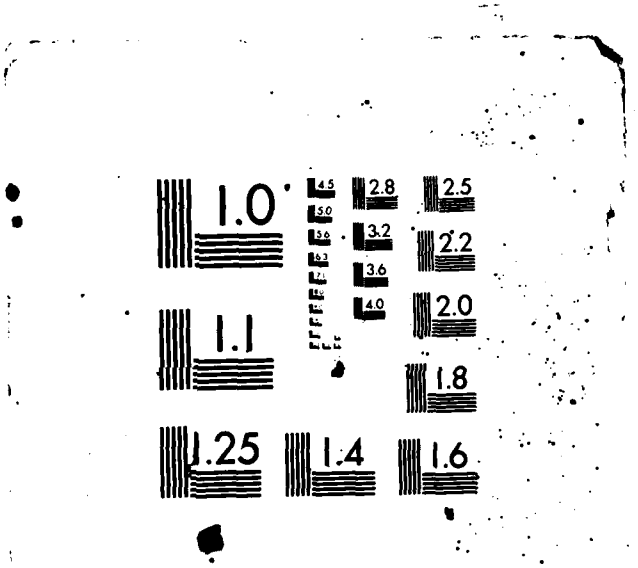

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RADC-TR-86-69
Final Technical Report
July 1986

SIGNAL PROCESSING CIRCUIT DEVELOPMENT

Northeastern University

Basil L. Cochrun

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This final technical report covers the development of electronic circuitry for operation of an IRCCD Camera using a 39,040 Schottky diode detector focal plane. The focal plane is an interline transfer CCD having a 160 (horizontal) by 244 (vertical) pts; photo diode matrix. The camera system consists of a sensor head and a signal processing unit. Both packages are small enough to satisfy airline requirements for carry-on luggage.

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PREFACE

This final technical report describes work performed at the Dana Research Center, Electronics Research Laboratory, Northeastern University, Boston, Massachusetts, from May 1983 thro ·jh ~~30~~ SEPT. 1985, under contract No. F19628-83-C-0087 with RADC. The principal investigator was B.L. Cochrun.

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SECTION I

INTRODUCTION

This final technical report covers the development of electronic circuitry for operation of an IRCCD camera using a 39,040 Schottky diode detector focal plane and peripheral circuitry related to the initial and final design. The entire system consists of two packages each of which is small enough to satisfy the airline requirements for carry on luggage.

The camera focal plane is an interline transfer CCD having a 160 (horizontal) by 244 (vertical) PtSi photodiode matrix which was designed by Walter Kosonocky of the RCA Sarnoff Laboratories. The camera system consists of a sensor head and a signal processing unit. The sensor head was designed by Doctor W. Ewing of RADC at Hanscom AFB Bedford, MA. This report is concerned primarily with the signal processing unit.

A simplified block diagram of the overall camera system is shown in Figure 1. Figure 1a is a block diagram of the sensor head pictured in the photographs of Figures 2-4. The second package containing the digital-analog signal processing unit (SPU) is shown as a block diagram in Figure 1b. It consists of five S100 plugin boards and two PC boards, one for the A/D circuitry and the other for the D/A circuitry. A third PC board serves to interface the front panel controls and the various boards.

The basic operation of this camera is for the most part the same as that for the 64x128 camera[1]. The sensor head, in particular, for either camera requires only a different digitial board to account for the difference in timing between the two focal planes. The circuitry outside the sensor head, the SPU, is similar to that for the earlier camera, however, the nonbinary number of rows and columns, 160x244, requires new circuitry and larger memories to achieve the features of pixel correction, background averaging and appropriate operation of the frame buffer memories.

The early design of the A/D board attempted to use the 12 bit DATEL 868 A/D with 500 ns conversion time and the Micronetworks MN37[illegible] T/H amplifiers with a typical acquisition time of 160 ns. These two devices represented state of the art in signal processing in terms of availability, speed, power consumption and reasonable cost. A careful analysis of the operating characteristics revealed that this combination just fell short of the

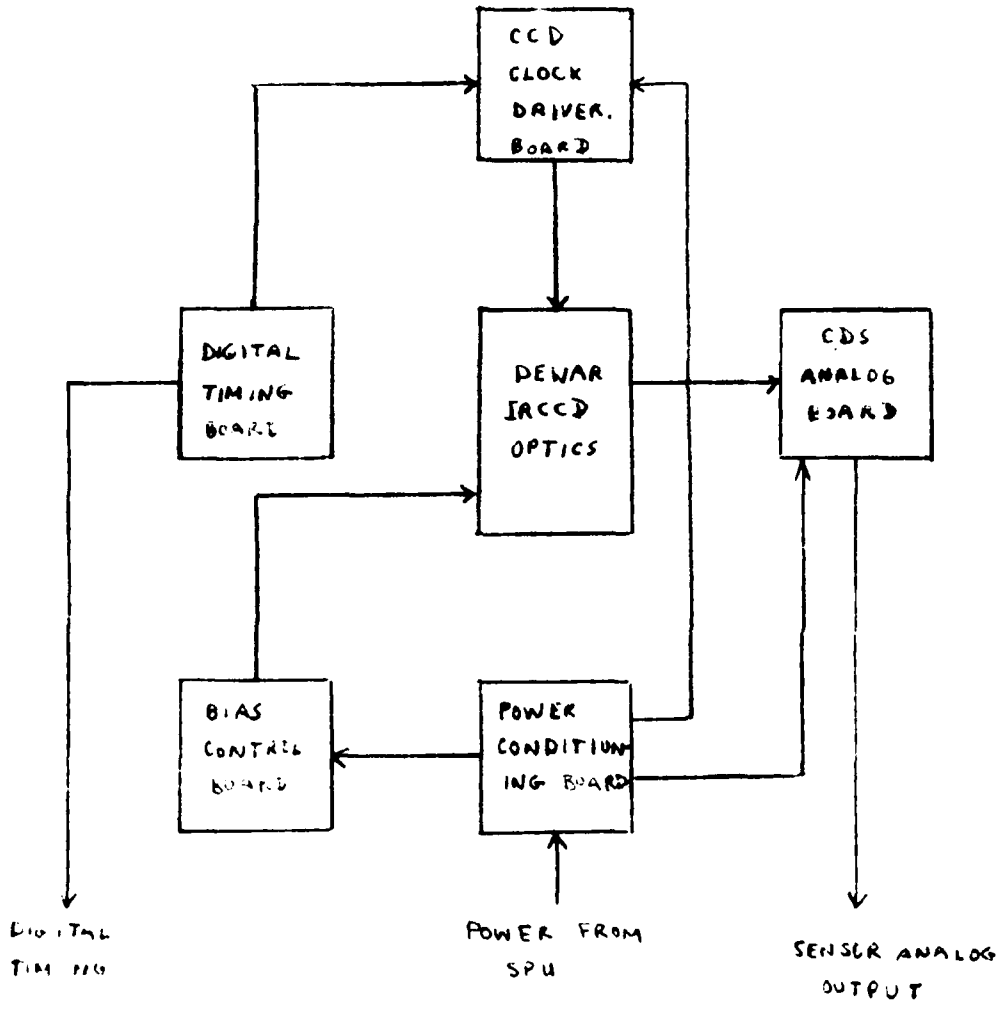


Figure 1a Simplified block Diagram of the Sensor Head

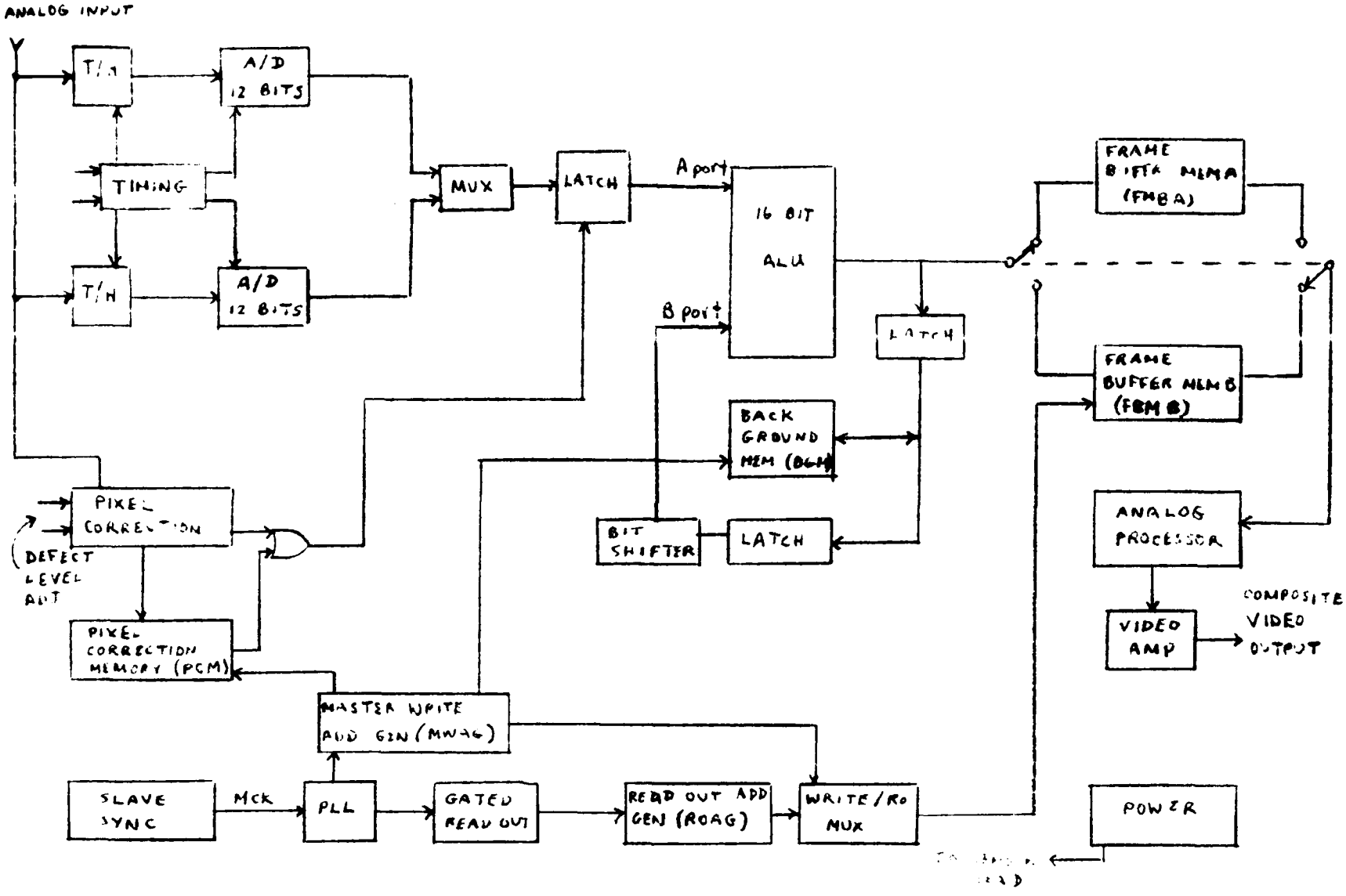


Figure 1b Simplified block Diagram of the Analog-Digital circuitry

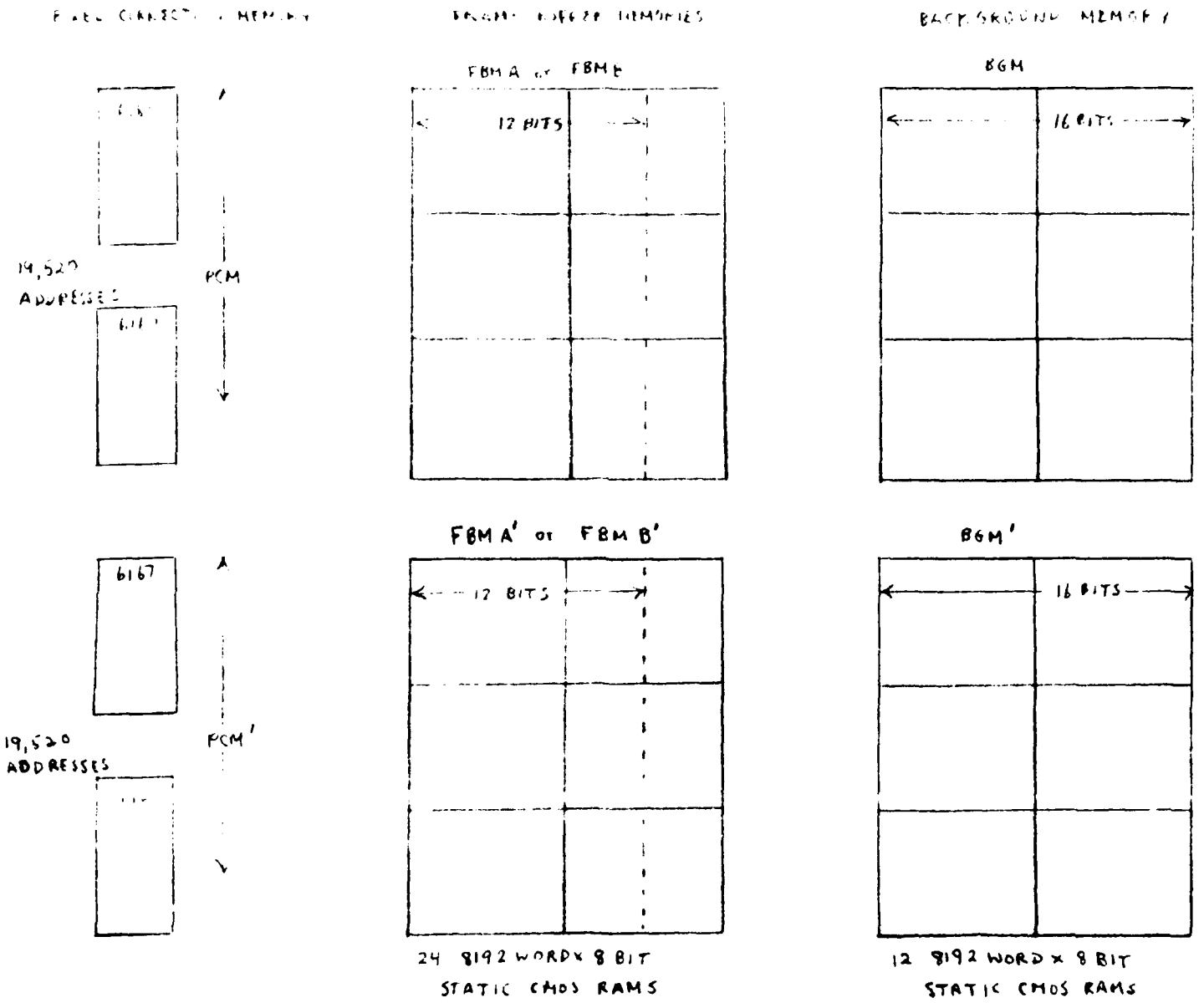


Figure 1c Three Memory Systems

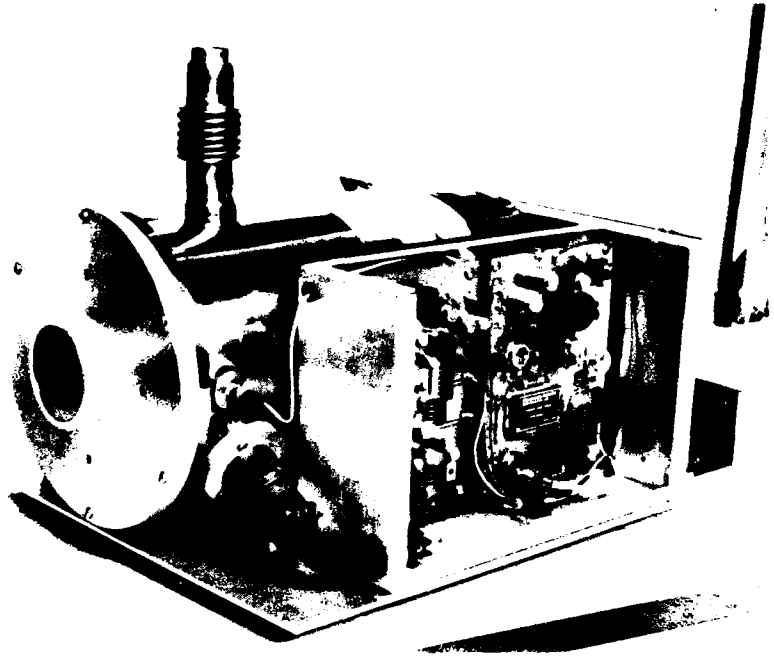


Figure 2 Sensor Head showing dewar and CDS PC board location

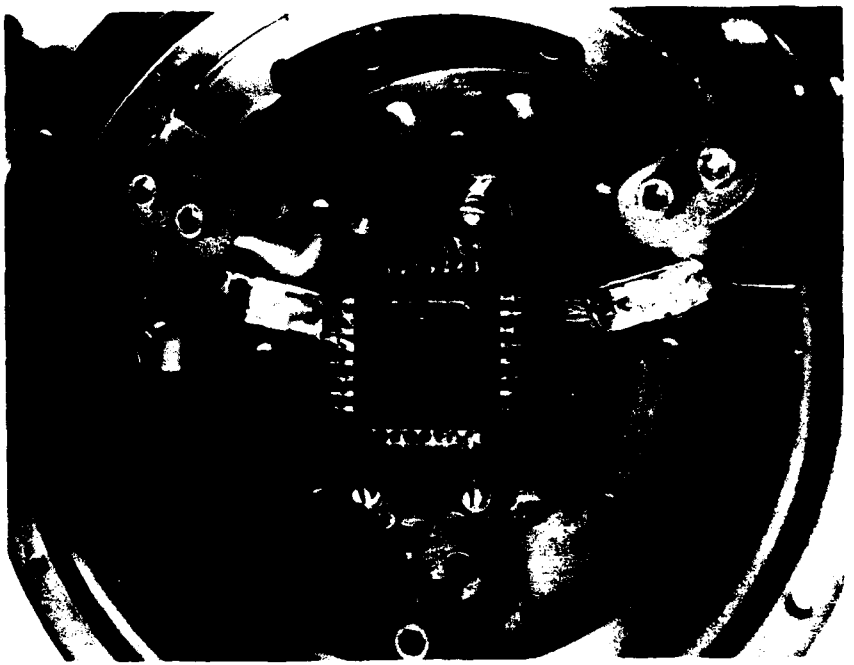


Figure 3 Sensor Head showing chip mounting behind the dewar

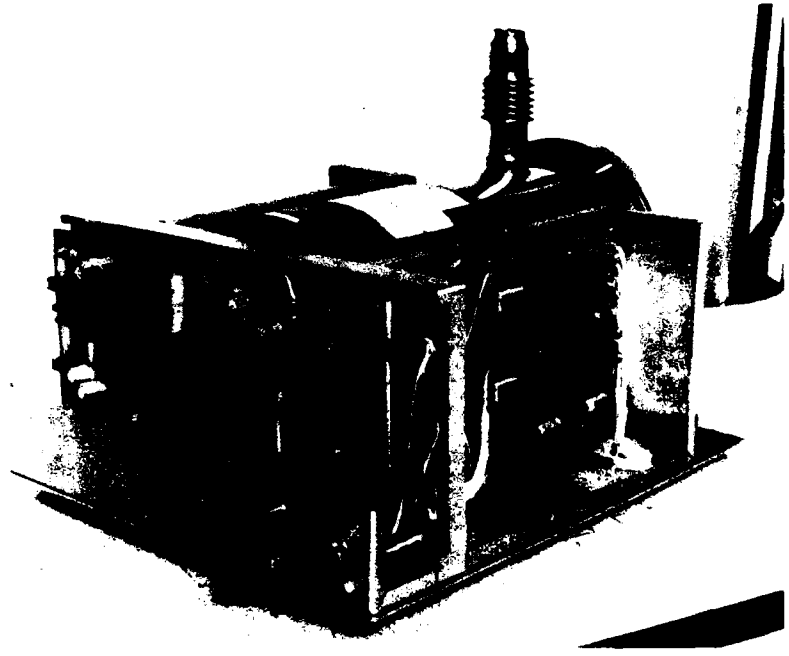


Figure 4 Sensor Head showing dewar, power regulator board and CCD driver PC board

necessary speed. Consequently, we made use of two Micronetworks MN5245 A/D's and two MN376 T/H's as indicated in Figure 1b.

Three memory systems are used, the pixel correction memory, (PCM), the background averaging memory, (BGM), and two frame buffer memories, (FBMA and FBMB). A simplified model for the organization of these is shown in Figure 1c. The PCM uses 6167 chips which are 16384x1 bit CMOS static RAM'S. The BGM and the FBM's use 5565 chips which are 8192x8 bit CMOS static RAM's. Twelve bit accuracy for the FBM's requires 6 chips for 122 lines or a total of 24 chips for both FBM's. The BGM during the background averaging operation involves 16 bit accuracy. Consequently the BGM requires 12 chips giving a total of 36 5565 memory chips for the entire system.

A preliminary explanation of the PCM operation is as follows. A comparator, controlled on the front panel, sets the allowable window for the pixel output level. If a pixel output falls outside the defect level a logic "0" is stored in the PCM. All other outputs are stored as logic "1's". At a constant ambient input the PCM is written for one frame. In normal operation when the PCM output is a zero the logic on the A/D board latches the A/D output to the data from the previous pixel output. When the PCM output is a "1" the output of the A/D is fed directly to the "A" ports of the ALU for processing.

The BGM is used to obtain a 12 bit 16 frame pixel by pixel average of the sensor data. This is achieved using a 16 bit hard wired ALU with "A" and "B" input ports. The first step in this process is to bit shift the BGM to utilize its full 16 bits. The BGM is cleared and with the ALU set to the ADD mode the 16 frame pixel by pixel sum is obtained. The BGM is then bit shifted back to utilize only the upper 12 bits of data and to obtain the average background for each pixel. Corrected imagery is obtained by setting the ALU to the subtract mode. The background average is then subtracted from the incoming sensor data on a pixel by pixel basis.

The FBM's are operated in a ping pong manner in that one memory is being written as the other is being read out. In writing, all of the even lines are written consecutively into A or B memory followed by all the odd lines into A' or B' memory. During read out (RO) the entire contents of the primed and unprimed memories are readout alternately during one TV field. This RO is repeated for the next TV field. Consequently, the entire RO consists of approximately 488 lines per frame at the TV rate of 30 frames/

second.

The analog processing block of Figure 1b consists of an ECL D/A, HDS1240E, followed by switched gains of 1, 2, 4 and 8, a four quadrant multiplier, log compression, multiple pole active video filtering and black level control.

In what follows in this report an attempt has been made to clarify the discussion of circuit behavior by simplifying references to different types of IC's. For the most part high speed CMOS logic circuits have been used to reduce power consumption. In a few places Fairchild Advanced Schottky Technology (FAST) devices have proved to be beneficial. For some circuits it was necessary to use standard TTL, Schottky Low Power, or Schottky devices. In most cases inclusion of SN74 preceeding the device type will be omited. For example, SN74HC04 will be written as HC04, and the SN74HCT04 will become HCT04. For FAST devices only F is used, i.e., the hex inverter SN74F04 will be referred to as F04. Schottky devices will appear as S139, low power Schottky as LS14 and 120 for standard TTL devices.

A glossary of the acronyms used in this report follows.

GLOSSARY

Background Memory	BGM
Borrow	BO
Composite-Data-Latch	CDL
Correlated Double Sampling	CDS
Dynamic Field Balance Correction	DFBC
Even Field	EF
Field Drive	FD
Flip Flop	FF
Frame Buffer Memory	FBM
Gated Readout Clock	GROCK
Line Drive	LD
Load	L
Maximum Flat Magnitude	MFM

Master Clock	MCK
Master Memory Select	MMS
Master Write Address Generator	MWAG
Memory Selet (Q,D)	MS
Operational Amplifier	OA
Phase-Locked Loop	PLL
Pixel Correction Memory	PCM
Readout	RO
Readout Address Generator	ROAG
Select	SEL
Signal Processing Unit	SPU
Start Convert	SC
Status	ST

SECTION II

CAMERA CIRCUITRY DETAILS

A. Sensor Head

Digital synchronization of signals and analog data used in the SPU originate in the sensor head. The primary source of timing is a 12.915 MHz crystal controlled oscillator located on the digital board shown in Figure 1a. An equally important chip is the Ferranti TV Synchronizing Pulse Generator chip ZNA134J. A block diagram of this chip is shown in Figure 5. This is the master synch chip which generates all of the control signals necessary for TV monitor presentation of video data. Figure 6 indicates the various output available from the ZNA134J.

A simplified derivative diagram of the digital board is shown in Figure 7. The digital board supplies to the SPU the following signals: XFR, T/H (160 pulses/line), a Master Clock (MCK), Even Field (EF), and the Line Drive (LD). The latter three signals are used to synchronize a slave ZNA134J chip in the SPU. The MCK signal of 2.583 MHz, required by the TV synch generator, is derived by dividing the 12.915 MHz crystal clock by five.

The transfer pulse (XFR) occurs every 16.67 milliseconds. Sandwiched between XFR pulses are the data readouts, alternately all the 122 even rows followed by all the 122 odd rows. This analog data is processed on the Correlated Double Sampling (CDS) board before reaching the A/D board in the SPU.

Earlier work using CDS circuitry had demonstrated its efficacy in noise reduction prior to digitizing analog signals.[2,3] The CDS circuit board in Figure 1a incorporates improvements over the circuitry reported on in references 2 and 3. Figure 8 illustrates the basic features of the initial design of the CDS circuitry used in the sensor head. In the final design the BUF 03's were eliminated. The reference voltage switching using SD210 and SD215 MOSFET's affords faster switching and the REF02 circuitry results in a more stable offset reference voltage. The MN376 T/H amplifier gives significant improvement in switching time, acquisition and settling times over the HTC0300 devices used earlier.

The CCD C clock rate is 6.4575 MHz. The chip output data rate, the pixel or CCD rate, is 1/4 of the C clock rate or 1.6144 MHz giving 619ns/pixel. This time is allotted as approximately 150 ns for reset and

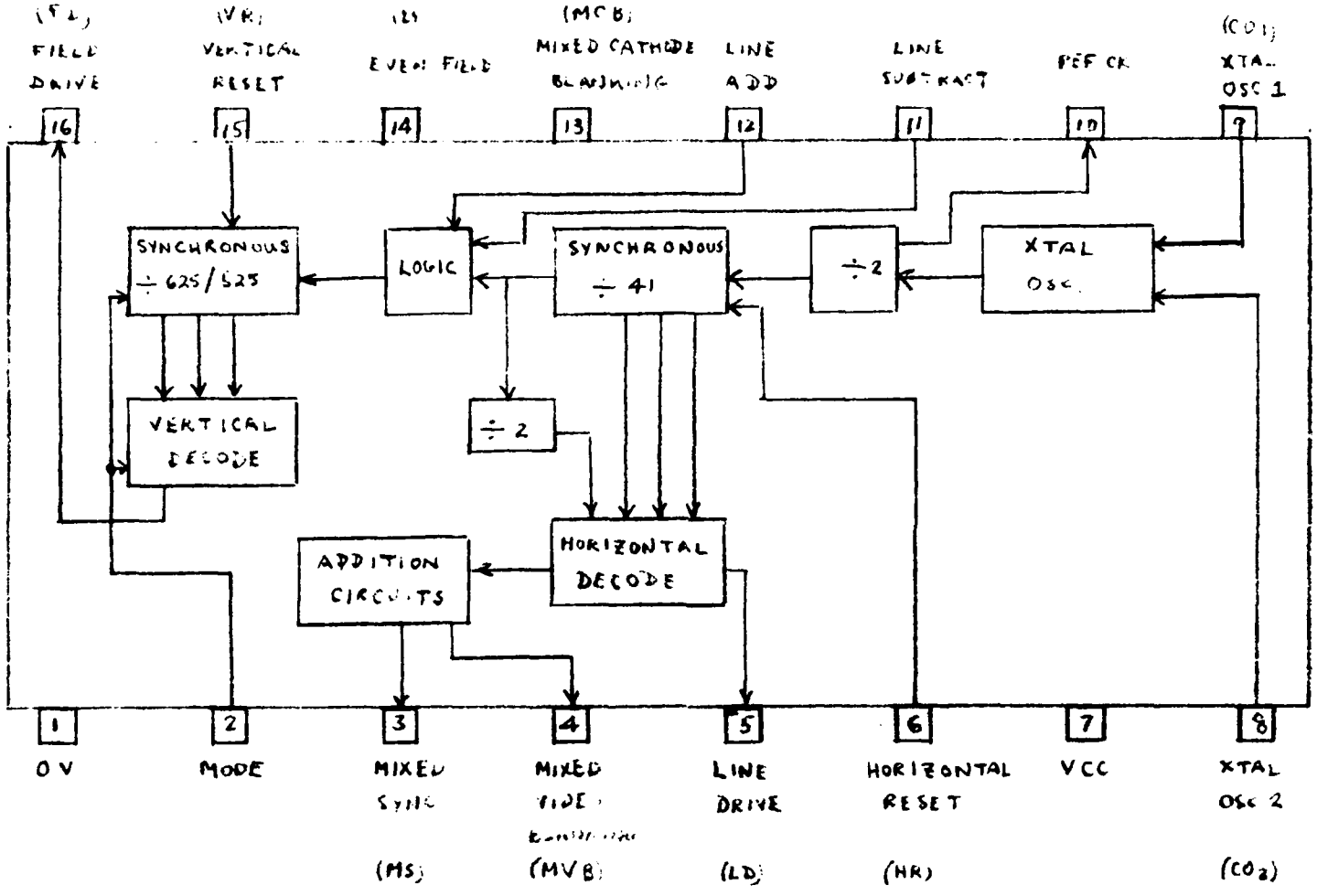


Figure 5 Block diagram of ZNA134J synch chip

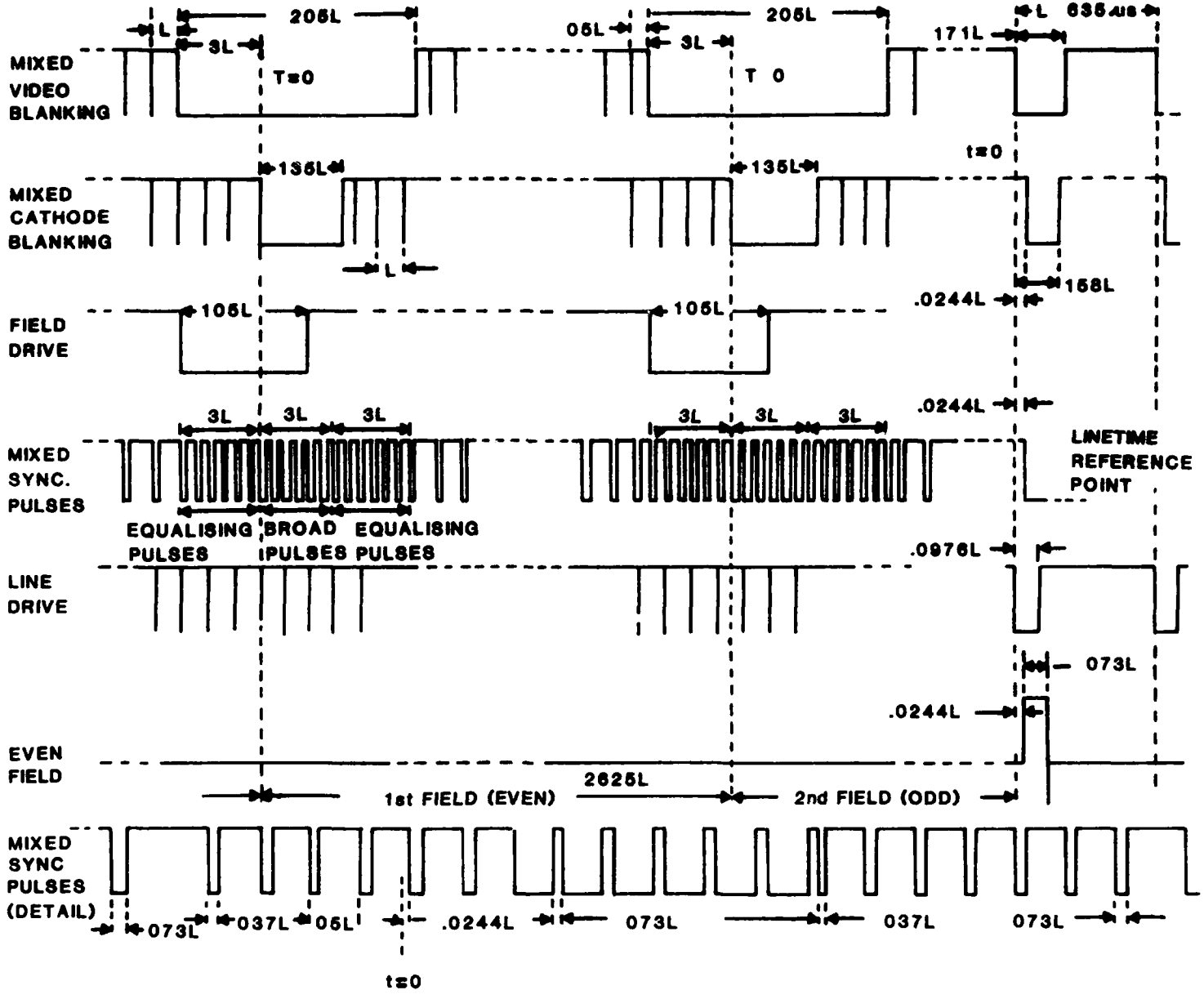


Figure 6. Waveforms for ZNA134 I.C. chip

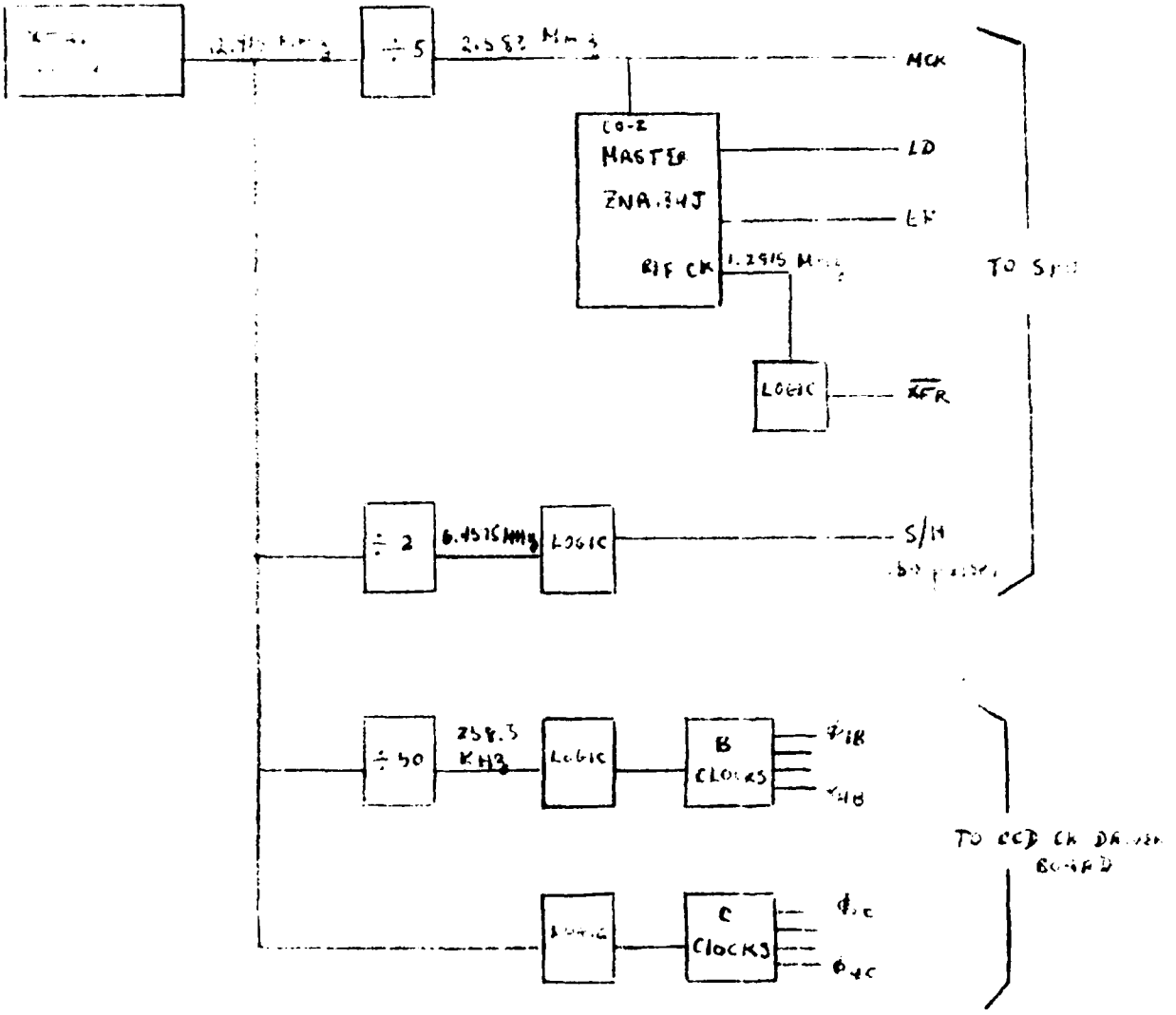


Figure 7 Simplified derivative diagram of digital board

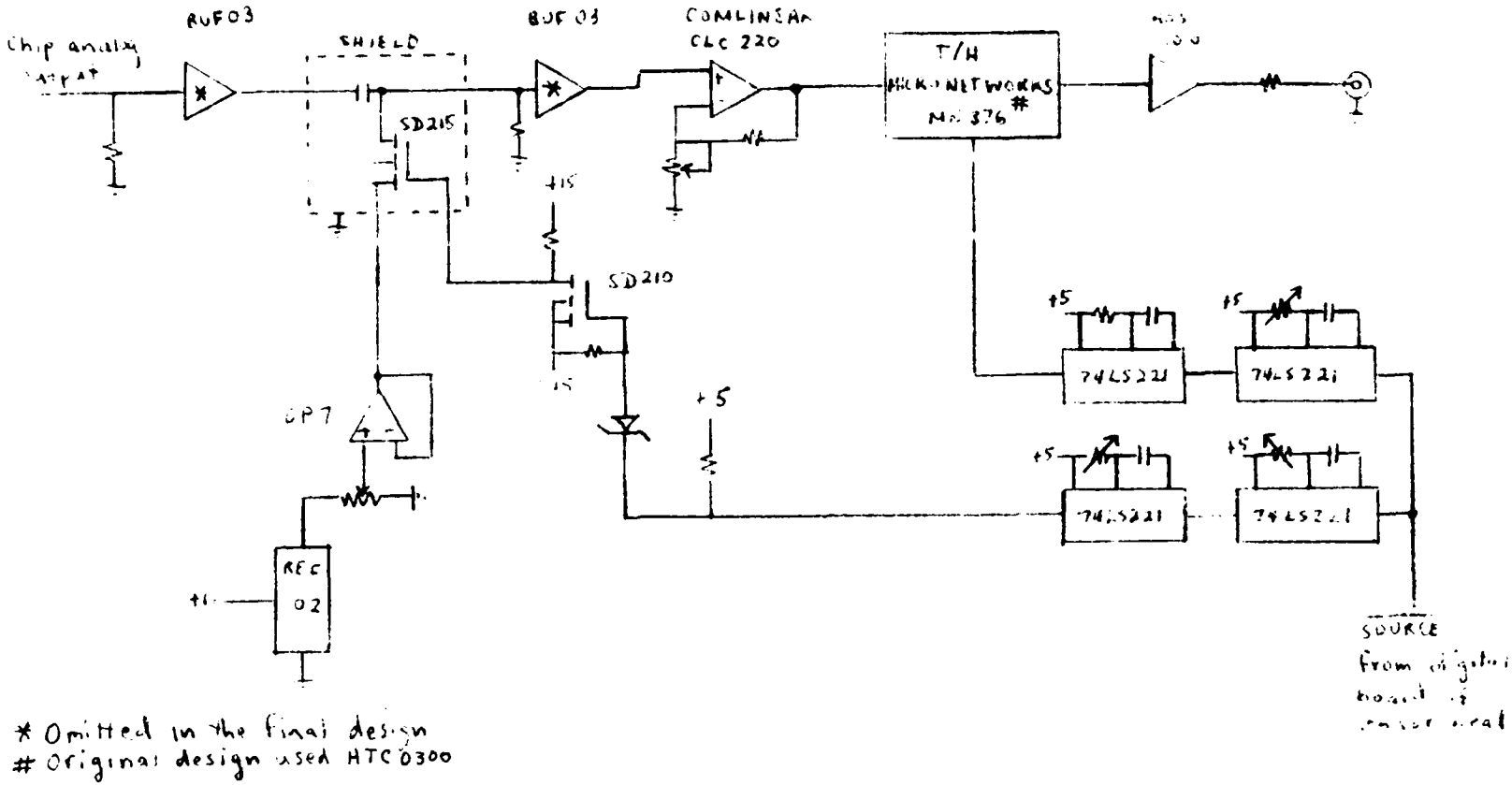


Figure 8 Improved CDS circuitry

approximately 450 ns for the S/H interval.

B. Signal processing Unit (SPU)

The SPU consists of an input A/D board, five S100 boards for processing the digital data and a D/A board to process the video output. The RO rate is determined on the basis of 488 lines/TV frame. The individual frame buffer memories ((FBM's), are readout completely (244 lines) once during each even TV field and once during each odd TV field. Since each TV field interval is 16.67 milliseconds, then 488 lines will be readout in 33 milliseconds at a TV frame rate of 30 frames/second. The interval between LD pulses - see Figure 6 - is 63.5 μseconds. Allowing 11.5 μseconds for horizontal blanking gives 52 μseconds/video line. Each chip row contains 160 pixels, thus, $52 \times 10^{-6}/160$ pixels = 325 ns/pixel or a video rate of 3.077 MHz. This rate determined the design of the phase-locked loop (PLL) controlled gated readout clock (GROCK).

A master write address generator (MWAG) is used for writing all three memory systems. This circuitry is synchronized with the $\overline{\text{composite-data-latch}}$, $(\overline{\text{CDL}})$, on the A/D board. The MWAG generates the memory control signals and the increment pulse INC to clock the write address counters.

1. A/D Board Timing Circuitry

The basic approach to digitizing the analog signal is indicated in Figure 1b. The box labelled "Timing" represents the circuitry necessary to generate "hold" pulses for operation of the T/H amplifiers. Each T/H amplifier is activated on everyother "hold" pulse. Each "hold" pulse is delayed by 100 ns to obtain the Start Convert (SC) pulse for the A/D's. A detailed schematic for the "timing" circuitry is shown in Figure 9. Waveforms for this circuitry are shown in Figure 10.

In Figure 9 the dual pulse synchronizer/driver chip SN74120 is a unique circuit that is used extensively in the SPU. As indicated in Figure 9 the 120 is capable of either single output pulse or pulse train operation. The wiring of Figure 9 suggests pulse train operation, however, the S/H pulse rate, the width of the S_1 pulses and the additional circuitry results in $\overline{Y}_1$ and $\overline{Y}_2$ having an output synchronized with everyother S/H pulse.

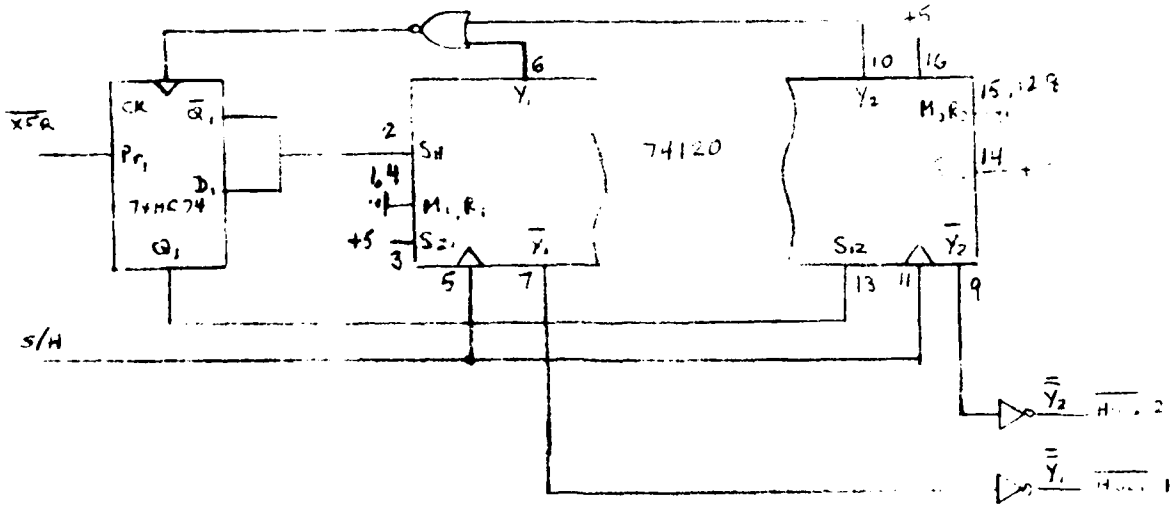


Figure 9 "Timing" circuitry of Figure 1b

In Figure 10 the $\overline{XFR}$ pulse at t = 0 presets $\overline{Q}_1 D_1$ low. With S_{11} low Y_1 will have an output pulse corresponding to the first S/H (CK120) pulse. Prior to the first S/H pulse both Y_1 and Y_2 were low and CK(74), the output of the NOR gate, is high. The positive pulse at Y_1 drives CK(74) low for the interval of the Y_1 pulse. At the end of the Y_1 pulse the first rising edge of CK(74) reverses the levels of S_{11} and S_{12}. Now with S_{12} low Y_2 will have an output for the second S/H pulse. S_{11} being high inhibits the Y_1 output. Next the trailing edge of Y_2 generates a rising edge to again clock the "D" type FF, reverse the levels of S_{11} and S_{12} and activate Y_1. Thus, the period of $\overline{Y_1}$ and $\overline{Y_2}$ is 1/2 that of the S/H pulse CK(1-0).

The remainder of the basic A/D circuitry is shown in Figure 12. The MICRONETWORKS MN 376 is a 12 bit linear T/H amplifier with a 200 ns maximum acquisition time and 100 ns settling time. The MN 5245 is a 12 bit A/D converter with 900 ns maximum conversion time and a 1 MHz conversion rate.

For the MN 5245 the minimum start convert (SC) pulse width is 50 ns and SC must remain low during conversion. The status (ST) pulse rises to a logic "1" 50 ns after the falling edge of SC. Digital output data from the previous conversion is valid typically 100 ns after the falling edge of SC and 40 ns after the rising edge St. Output data becomes valid on the falling edge of ST. These characteristics for the MN5245 are shown at the top of Figure 11 which indicates idealized waveforms for the A/D operation.

In Figure 12 circuit details for the remainder of the A/D board are shown. The digitized data from the two A/D's is muxed to the HC273 latches by means of three HC157's. When the select (SEL) input is low the Y outputs are from A/D_1. Synchronization with the $\overline{XFR}$ pulse is achieved by "D" type FF_1. The $\overline{XFR}$ pulse drives CL_1 low and presets $\overline{Q}_1 D_1$ high. At the end of the next 70 ns pulse from the composite-data-latch circuity SEL goes low and data is selected from A/D_1. On the next 70 NS pulse data will be selected from A/D_2.

The remainder of the circuitry in Figure 12 is related to the pixel correction circuitry. This will be discussed in Section 35 for the PCM.

7. Slave Sync and Phase-Locked Loop (PLL)

A block diagram of the PLL is shown in Figure 13. The desired f_2 is

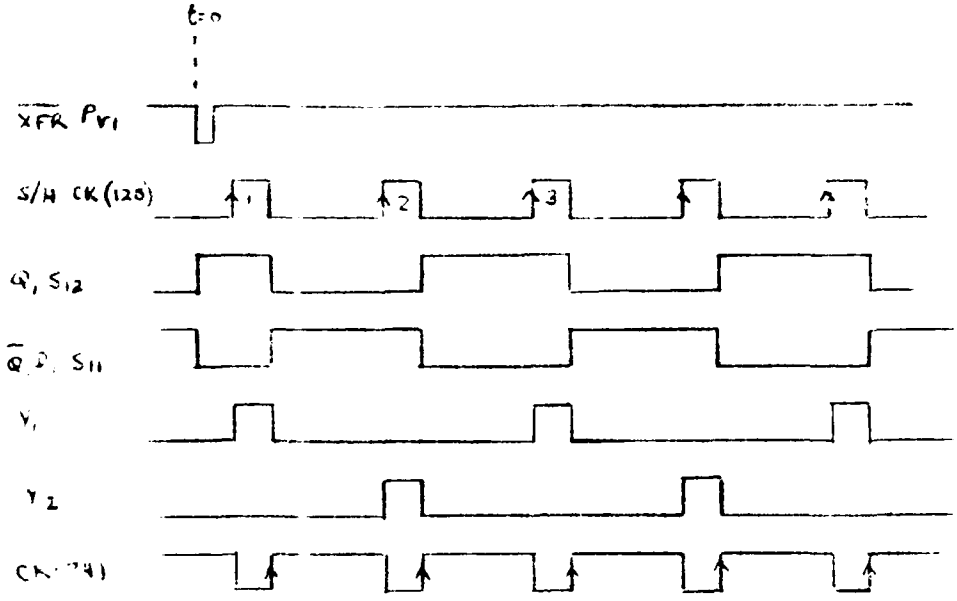


Figure 10 Waveforms for timing circuitry of Figure 9

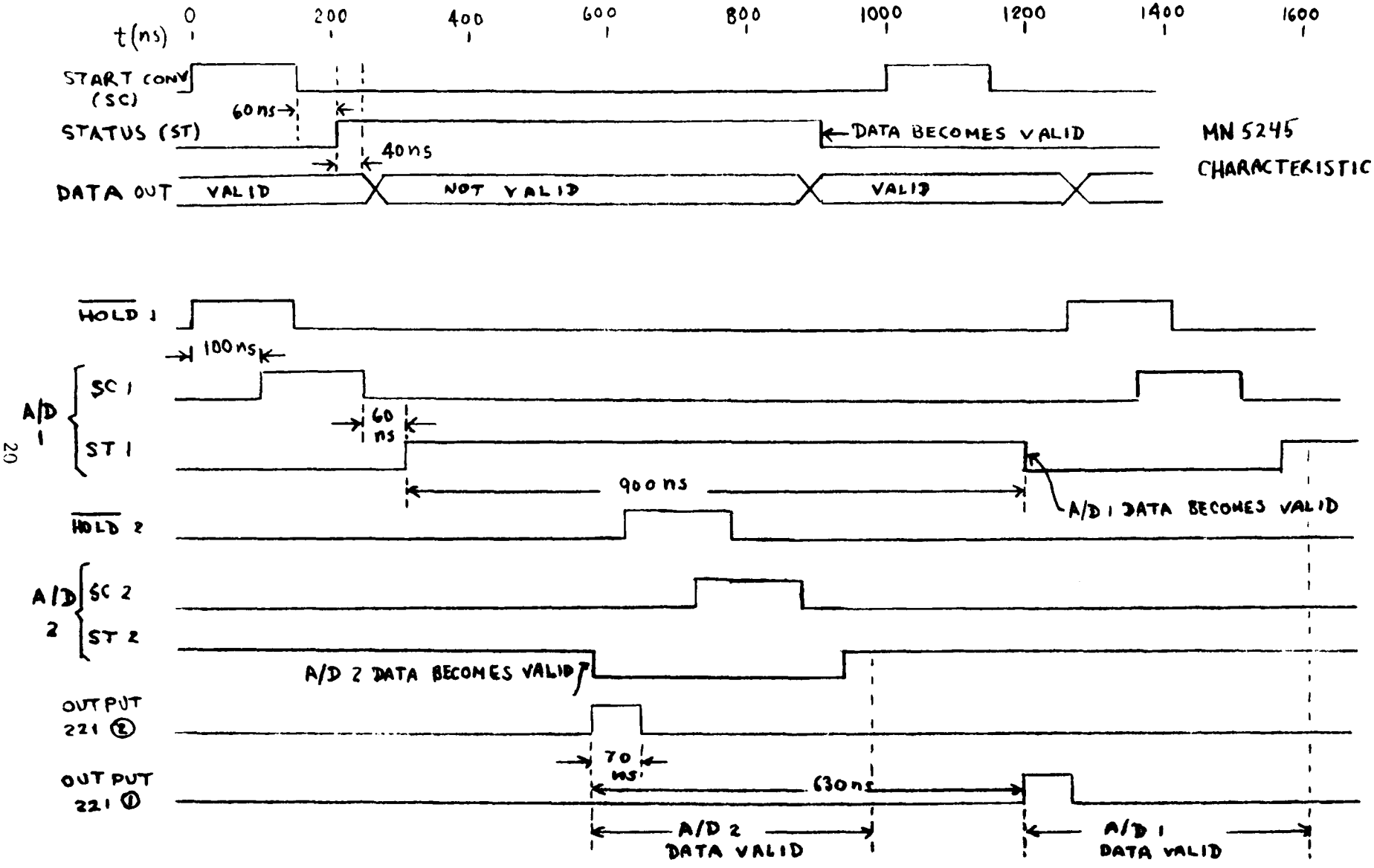


Figure 11 A/D timing diagram

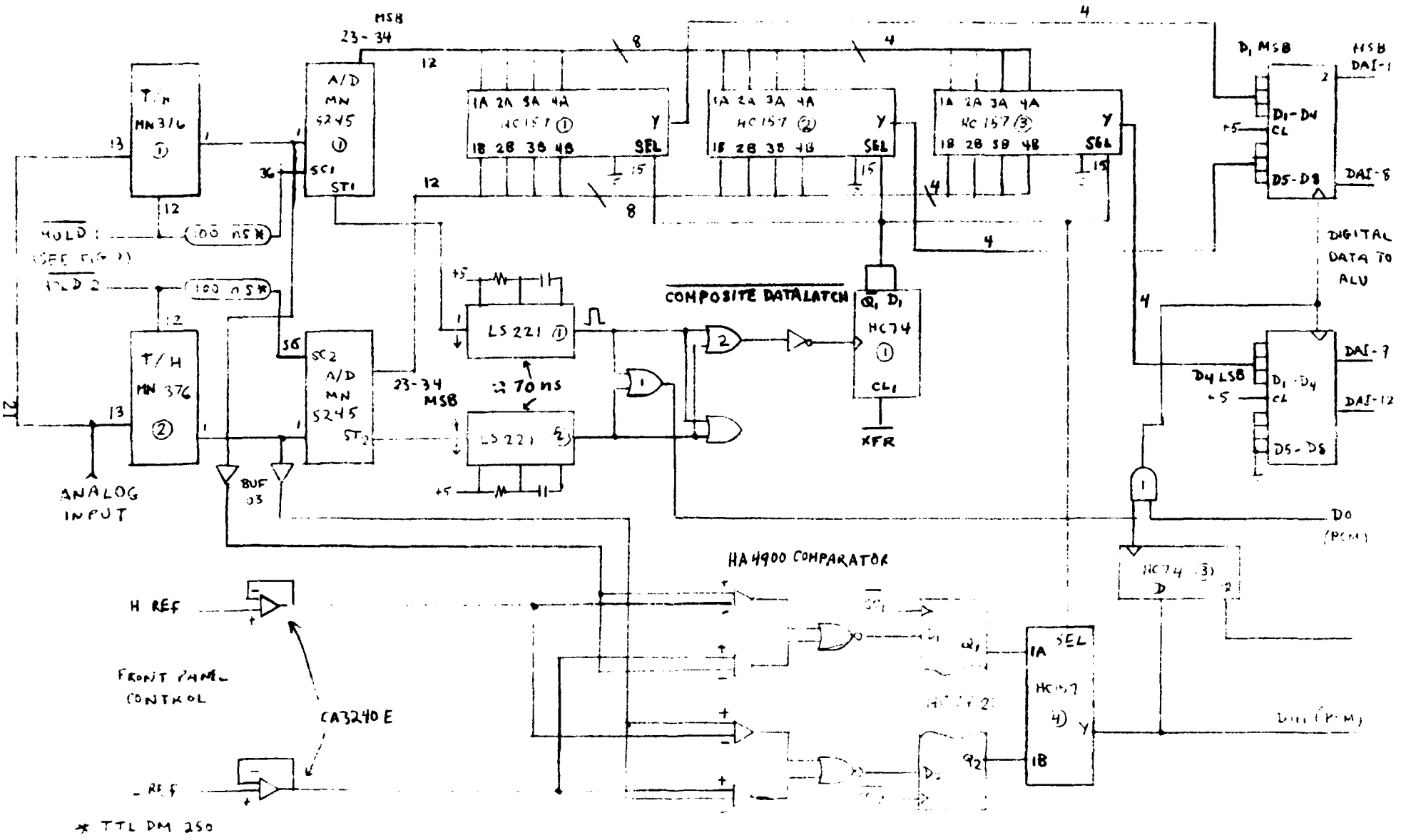


Figure 12 A/D board circuitry

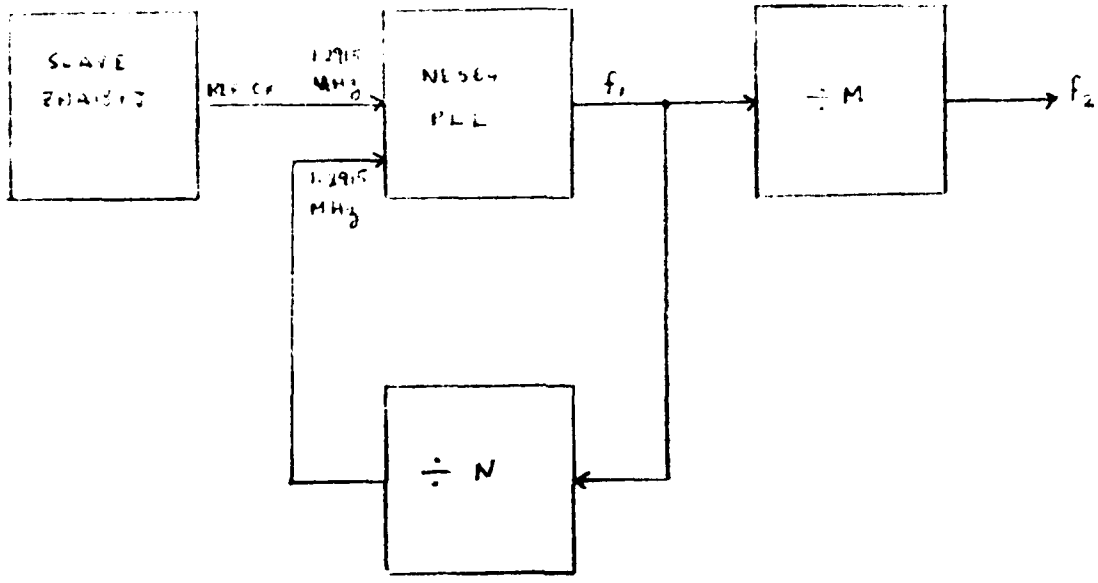


Figure 13 Phase-Locked-Loop (PLL) block diagram

$$f_2 = f_1/M$$

where

$$f_1 = 1.2915 \times 10^6 N$$

or

$$f_2 = 1.2915 \times 10^6 (N/M) = 3.077 \times 10^6.$$

Thus

$$N/M = 2.38 \text{ or approximately } 2.4 = 12/5.$$

Taking N = 12 and M = 5 gives

$$f_1 = 15.498 \text{ MHz and } f_2 = 3.0996 \text{ MHz.}$$

The rounding off of 2.38 to 2.4 gives 3.0996 MHz as compared to the initial value of 3.077 MHz, however, this only means that the 160 pulses required between LD pulses will occur in an interval somewhat less than the original specified 52 μs. Figure 14 shows the detailed PLL schematic. Division by 12 in the feedback loop is accomplished in two steps. The HC161 counter divides by 6 with an assymetric output to the HCT74 "D" type FF. The latter circuitry divides by two to obtain 1.2915 MHz with a 50% duty cycle.

3. Gated Readout Clock (GROCK)

The Grated Readout circuitry is required to obtain 160 pulses, each with a period of approximately 322 ns, sandwiched between succeeding LD

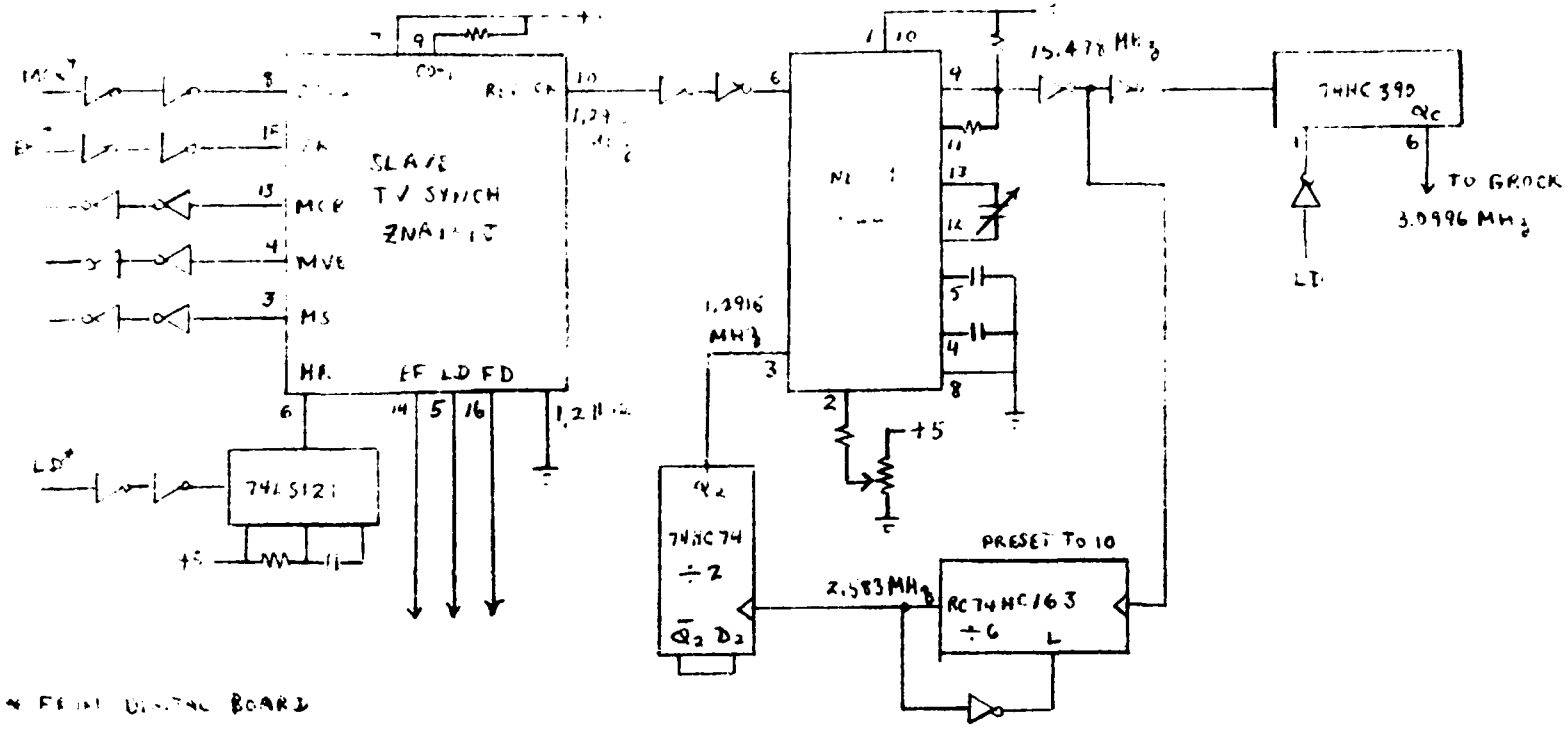


Figure 14 PLL schematic

pulses. This circuitry is shown in Figure 15 and the associated waveforms in Figure 16. The CK input for the 120 is 3.0996 MHz. The negative gate width for the S_2 control must be $160x1/3.0996x10^6$ or 51.6 s. The $\overline{LD}$ pulse width is 6.2 μs. The time between $\overline{LD}$ pulses is 63.5 s. Consequently there is an interval of 57.3 μs in which to fit the 160 gated pulses. The starting location after the $\overline{LD}$ pulse is set by approximately seven cycles of 1.2915 MHz using the HC161 counter and the $HC11_2$ AND gate. Approximately 5.4 μs after the $\overline{LD}$ pulse, CK_1 of the HC74 sets Q_a and S_2 low and Q_1 high which activates the HC161 counters and the output gate of the 120. After 160 counts of 3.0996 MHz the $NC11_2$ AND gate drives PR_1 low momentarily which terminates the 120 output gate and clears the HC161 counters.

The 5.4 μs interval after the $\overline{LD}$ pulse is not critical, however, the first gated pulse must always start at the same time. The clear for the HC390 counter - see Figure 14 - is synchronized with $\overline{LD}$. The 3.0996 MHz is synchronized with the PLL. Consequently, no difficulty was experienced with gate starting stability.

4. Master Write Address Generator (MWAG)

The MWAG is synchronized with the $\overline{\text{Composite-Data-Latch}}$,$(\overline{CDL})$, pulse from the A/D board as indicated in Figure 12. Circuit details of the MWAG are shown in Figure 17 and associated waveforms in Figure 18.

On the rising edge of the $\overline{CDL}$ pulse S_1 of the 120 is driven low by Q_1 of the "D" type FF HCT74 thereby initiating a train of pulses at the input CK rate of 15.498 MHz. At the same time the load input (L) of the HC192 counter rises having preset the counter to 1. Y_1 will continue to clock the counter until S_1 of the 120 rises. Q_D initiates this change by presetting the "D" type FF.

The counter outputs Q_B and Q_C of the HC192 with the appropriate logic shown in Figure 17 generates the necessary control signals for writing all three memories. Details of this circuitry will be discussed later in the appropriate sections.

The preset pulse for the "D" type FF is delayed and used as the CK input (INC) to increment the write address counters $HC161_1$ through $HC161_4$. These counters are initially cleared by the $\overline{XFR}$ pulse. After 19520 memory

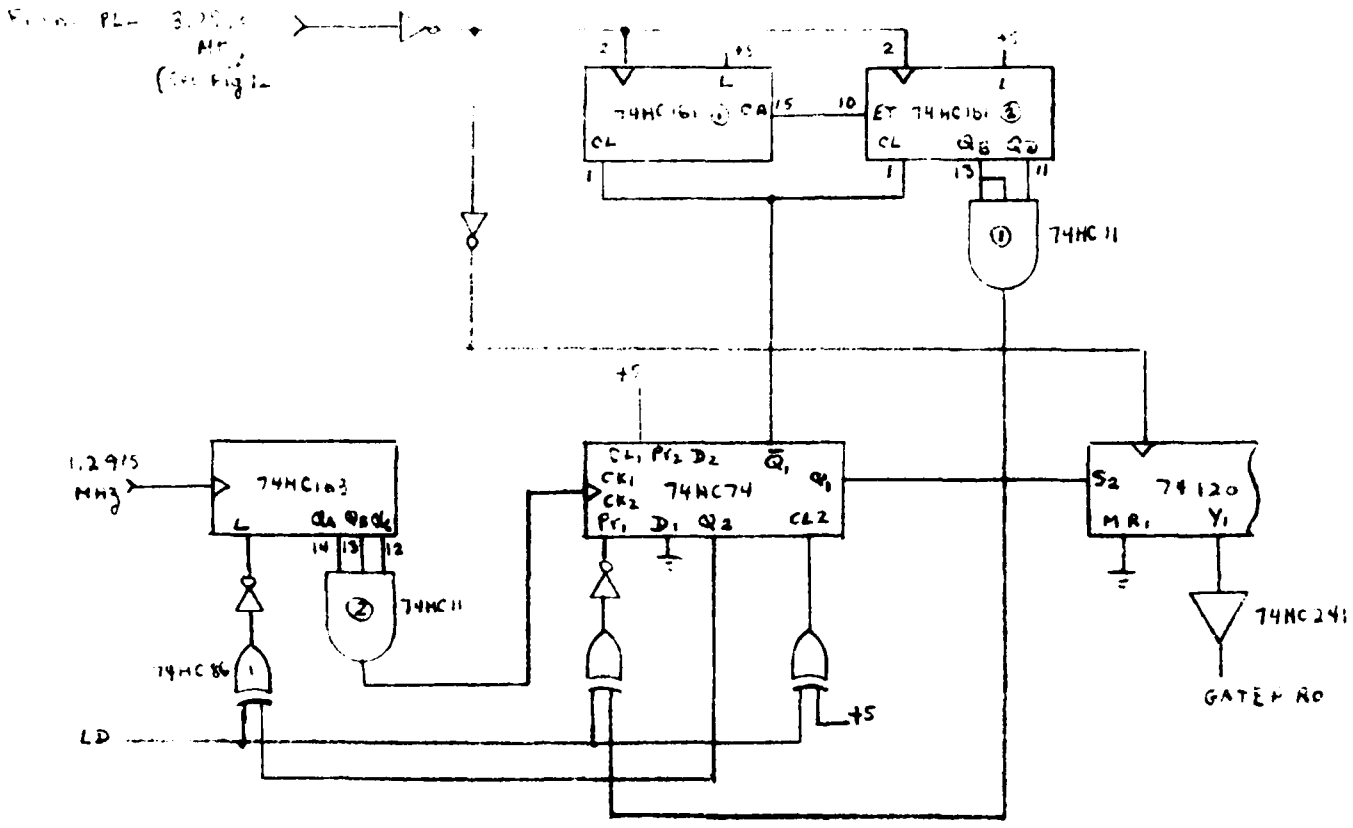


Figure 15 Gated Readout Clock (GROCK) circuitry

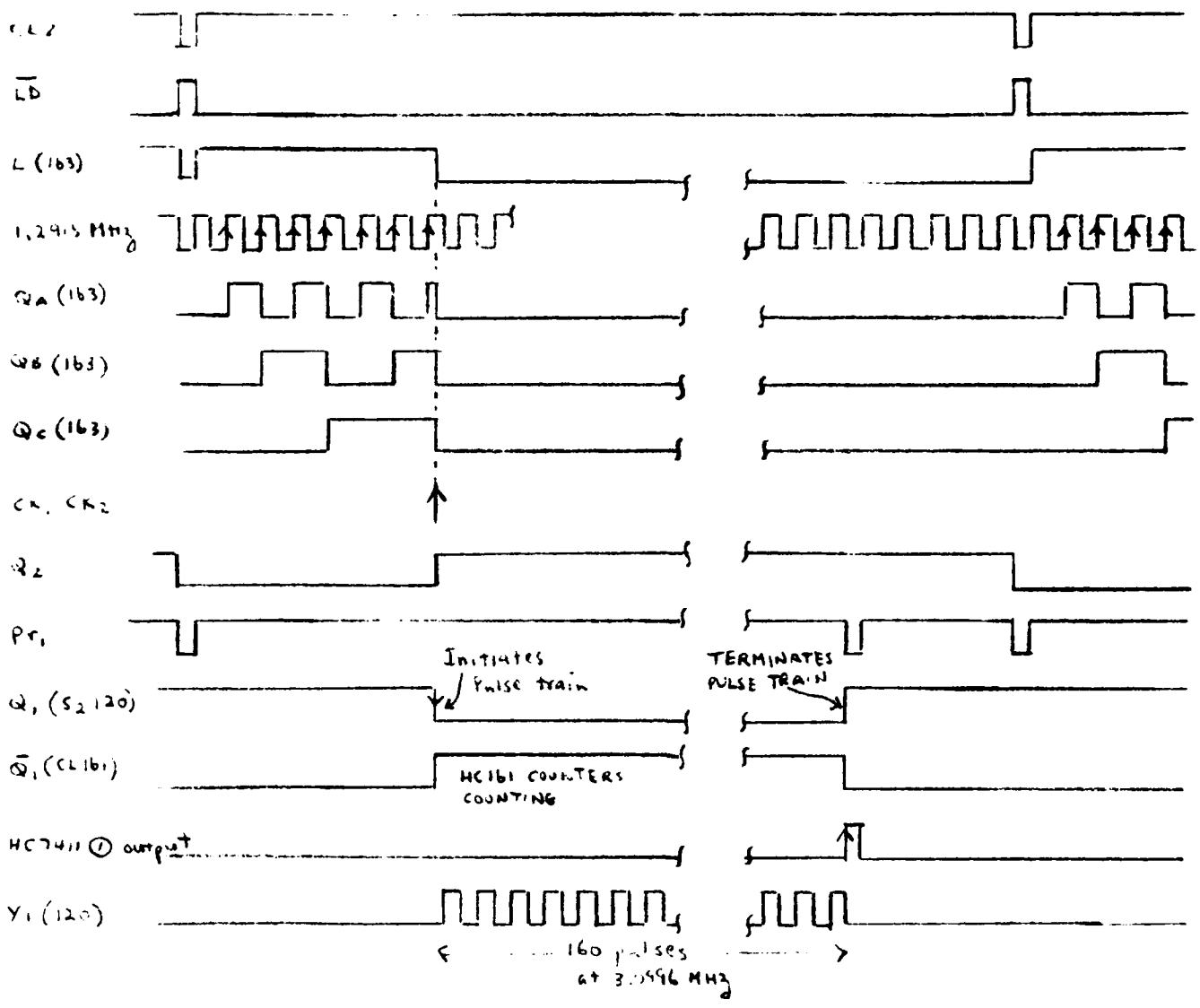


Figure 16 Timing diagram for GROCK

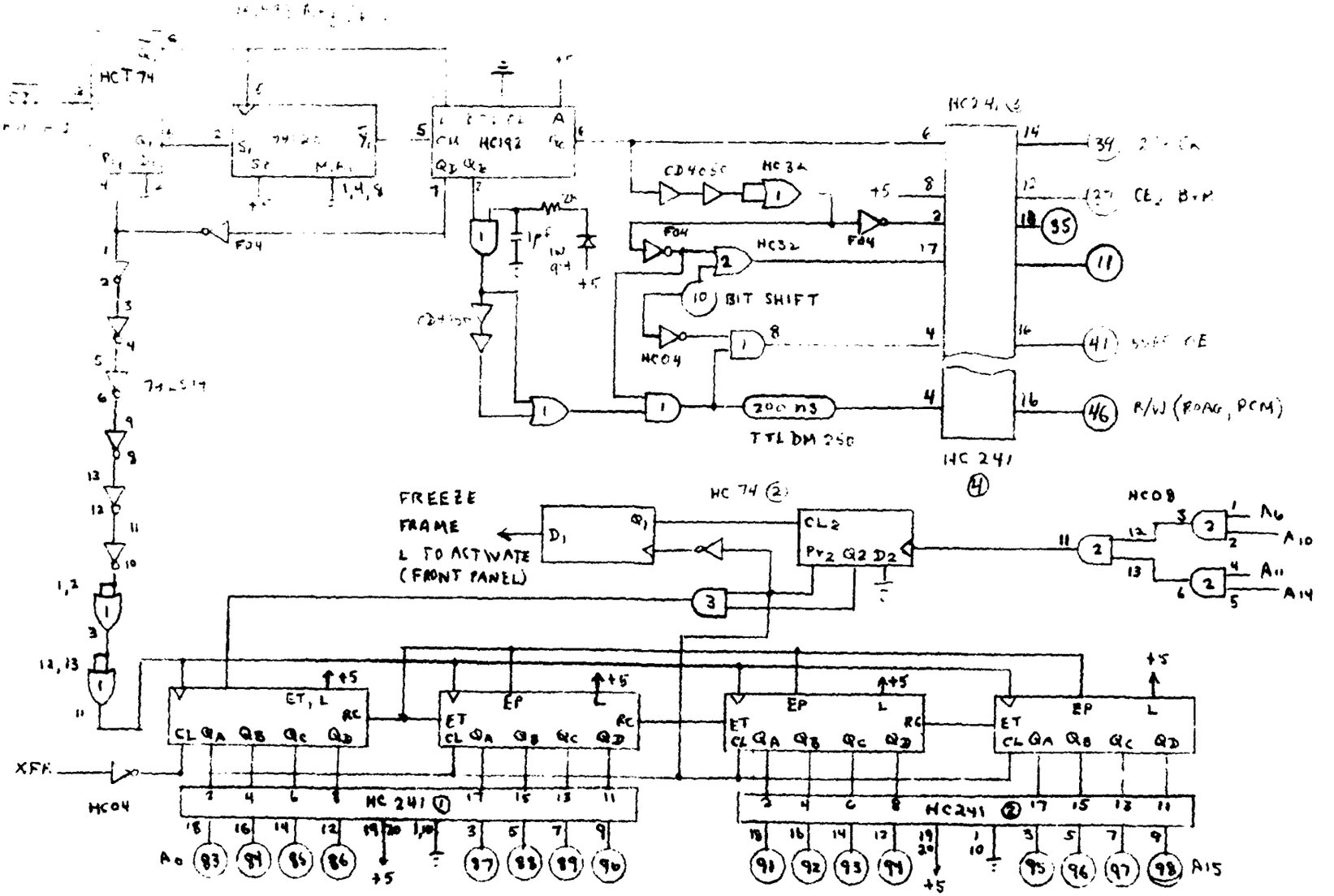


Figure 17 Master Write Address Generator (MWAG) circuitry

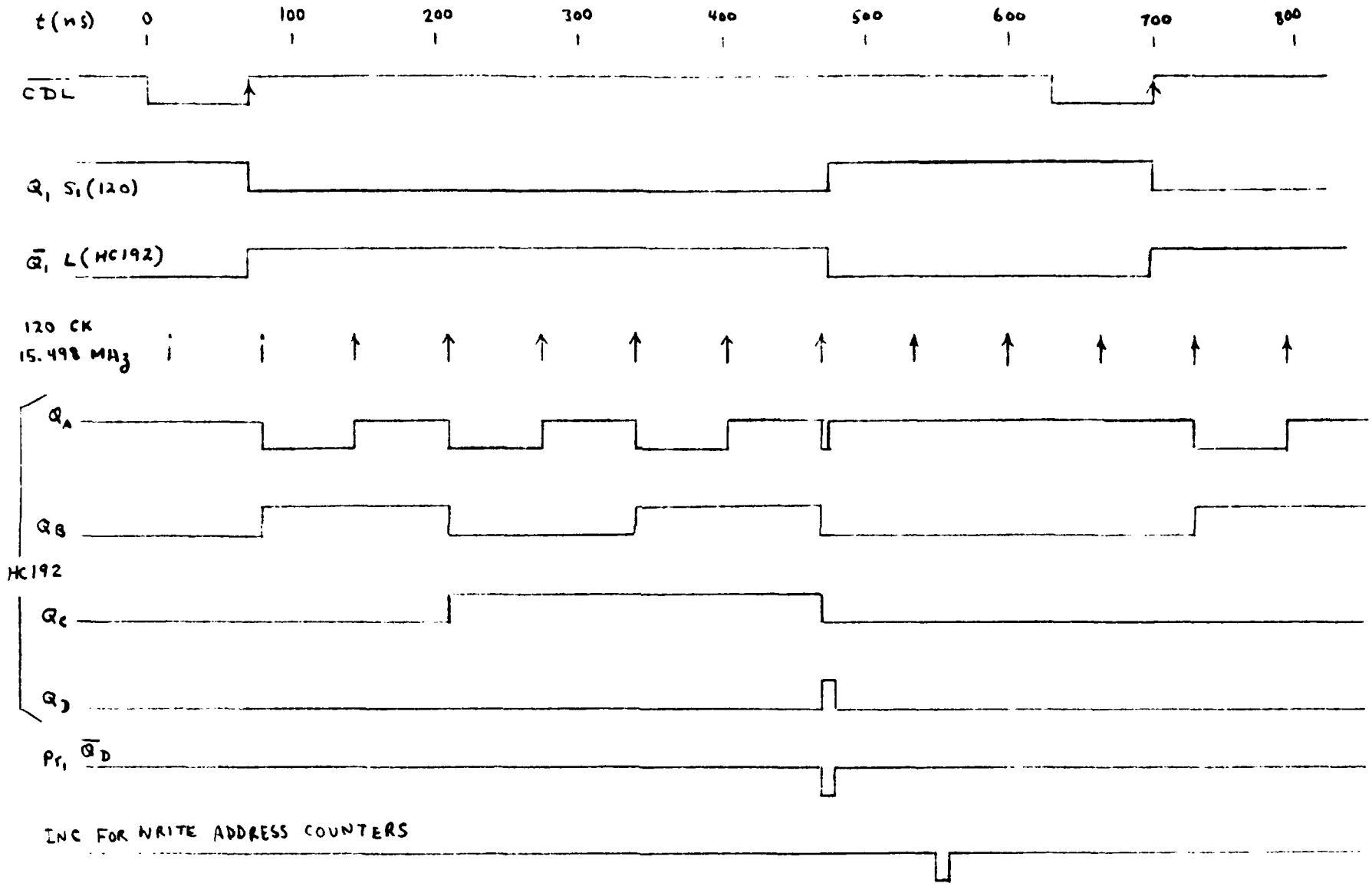


Figure 18 Timing diagram for MWAG

addresses, data for either the 122 odd or 122 even lines will have been written to the appropriate memory locations. The three AND gates in the lower righthand side of Figure 17 are connected to again clear the counters after 19520 increments and prior to the next $\overline{XFR}$ pulse. This clearing circuitry is not necessary, however, it is used as a precautionary measure to eliminate any possible noise contamination that might result from the readout of the unused memoryocations.

An important option for the camera is the capability of "freeze-frame" operation. The "D" type FF_2 in Figure 17 is used for this purpose. When D_1 is held low by the front panel switch, the output of AND gate 3 is held low. Since this output is EP of counter $HC161_1$, which must be high for counting, writing is inhibited. However, the data in the FBM's, valid before D_1 was made low, will continue to be readout. Once D_1 is again high normal operation will resume.

5. Pixel Correction Memory (PCM)

The basic function of the pixel correction circuitry is to substitute data from the previous pixel for any detector whose output does not fall within a presettable limit, ie., within the comparator window. The circuitry for this purpose is shown in Figures 12 and 1.

In Figure 12 the output of the comparator is normally at a logic "1" level. If the pixel output does not fall within the permissible level D_{in} is a logic "0". D_{in} to the PCM is obtained from the $HC157_4$.

The circuitry for controlling the PCM is indicated in Figure 19. The PCM control switch, located on the front panel, must be held low for one frame to completly load the memory. Four memories are used, two for the odd pixels and two for the even pixels. The differentation for the two sets is indicated in Figure 19 by the chip selects CS_1, CS_2, CS'_1 and CS'_2.

When pin 5 of $HC14_2$ is grounded by the PCM front panel switch a high output results for one input of all three AND gates. This is the write position. D_{in} from the A/D board is gated to the PCM memory input. The R/W signal - see Figures 17 and 18 - is gated by AND gate 2 and inverted to obtain the necessary negative $\overline{WE}$ pulse. The output from AND gate 3 gives the necessary negative $\overline{CS}$ pulse for the sequential chip select circuitry.

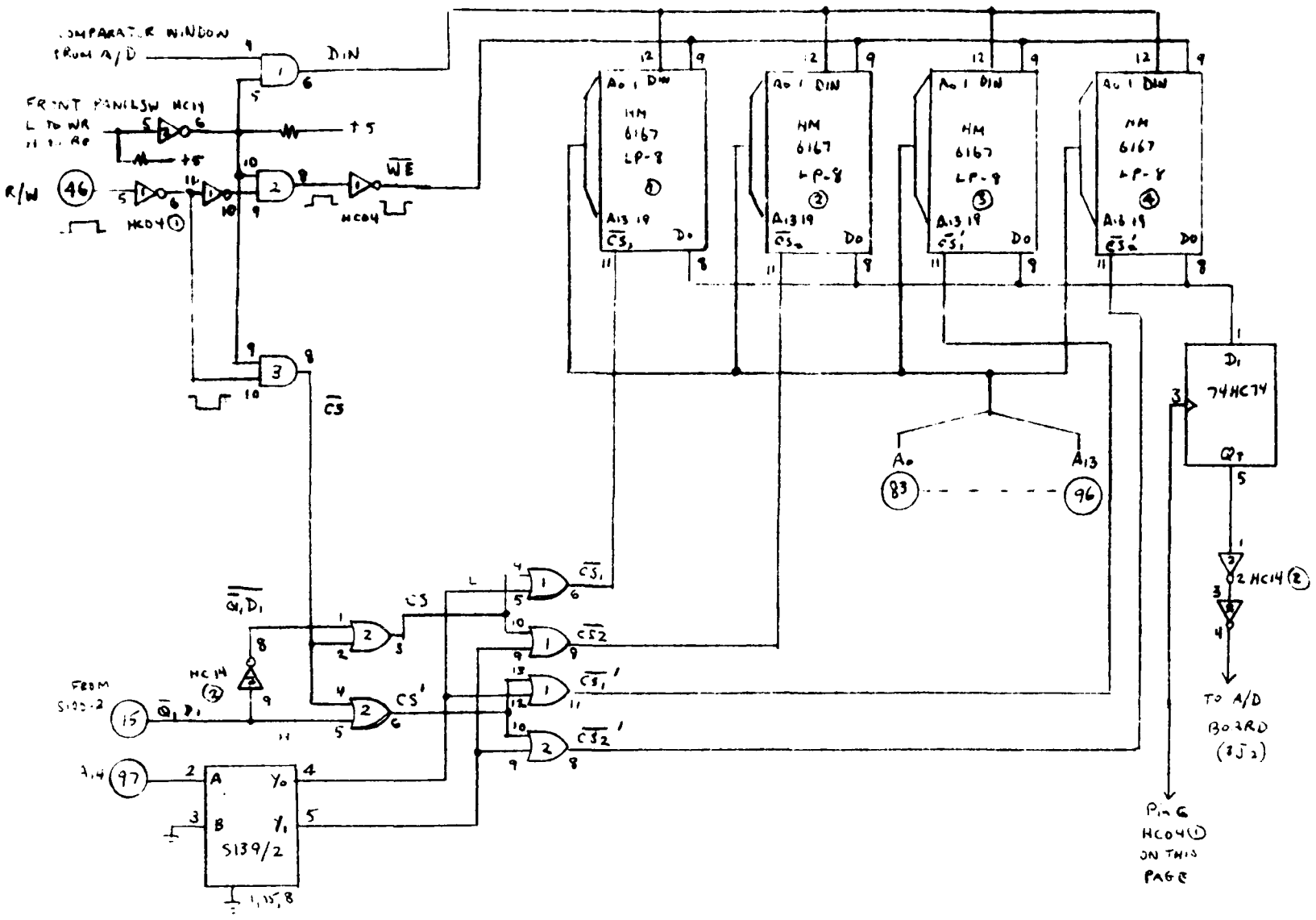


Figure 19 Pixel Correction Memory (PCM) circuitry

The $\overline{Q}_1 D_1$ input from the bus terminal 15 has not been discussed as yet. It is derived from the master memory select (MMS) circuitry discussed in section B7. It is a positive pulse of 16.67 milliseconds duration followed by a negative pulse of the same duration. If we assume that pin 5 of OR gate 2 is positive for 16.67 milliseconds the OR gates having outputs CS_1' and CS_2' will be held high for 16.67 milliseconds thus disabling memories 3 and 4. However, pin 1 of OR gate 2 will be held low for the same 16.67 milliseconds and $\overline{CS}_1$ and $\overline{CS}_2$, in conjunction with the rest of the logic circuitry, will sequentially enable memories 1 and 2.

After one frame with pin 5 of $HC14_2$ disconnected from the front panel switch all three AND gates will have a common low input. D_{in} will not be gated through to the memory inputs. The output of AND gate 2 will remain low with $\overline{WE}$ held high. This is one requisite for RO. The output of AND gate 3, $\overline{CS}$, is held low. Assume again that pin 1 of OR gate 2 is low. The decoder S139 will sequentially select the OR gates having outputs $\overline{CS}_1$ and $\overline{CS}_2$. Now with WE held high D_0 will set the D_1 level of the "D" type FF. This FF is clocked by the rising edge of the R/W pulse and the memory content D_0 will appear at the Q_1 output and thus reach the A/D board. Timing diagrams for writings and readout of the PCM are shown in Figure 20.

Referring to Figure 12, D is one input to AND gate 2. The other input is from OR gate 1. The output of AND gate 1 is the CK for the HC273's. If D_0 is a logic "0" there will be no clock pulse and with the CK input at a low level the outputs of the octal D latches will be Q_0 or the value of the previous output. On the otherhand if D_0 is a logic "1" the rising edge of the output from AND gate 1 will clock the current data from the A/D to the ALU "B" port inputs for processing.

c. Background Averaging and ALU Circuitry

A block diagram of the back ground averaging and ALU circuitry is shown in Figure 21. The ALU portion of Figure 21 consists of one 182 chip, and four 14 chips with input ports 'A' and 'B' and output port 'F'. Each port has four inputs. Thus the ALU and the BGM can operate at a 16 bit level during the averaging process.

The MUX serves to select the bit level input to the ALU "B" port. Data

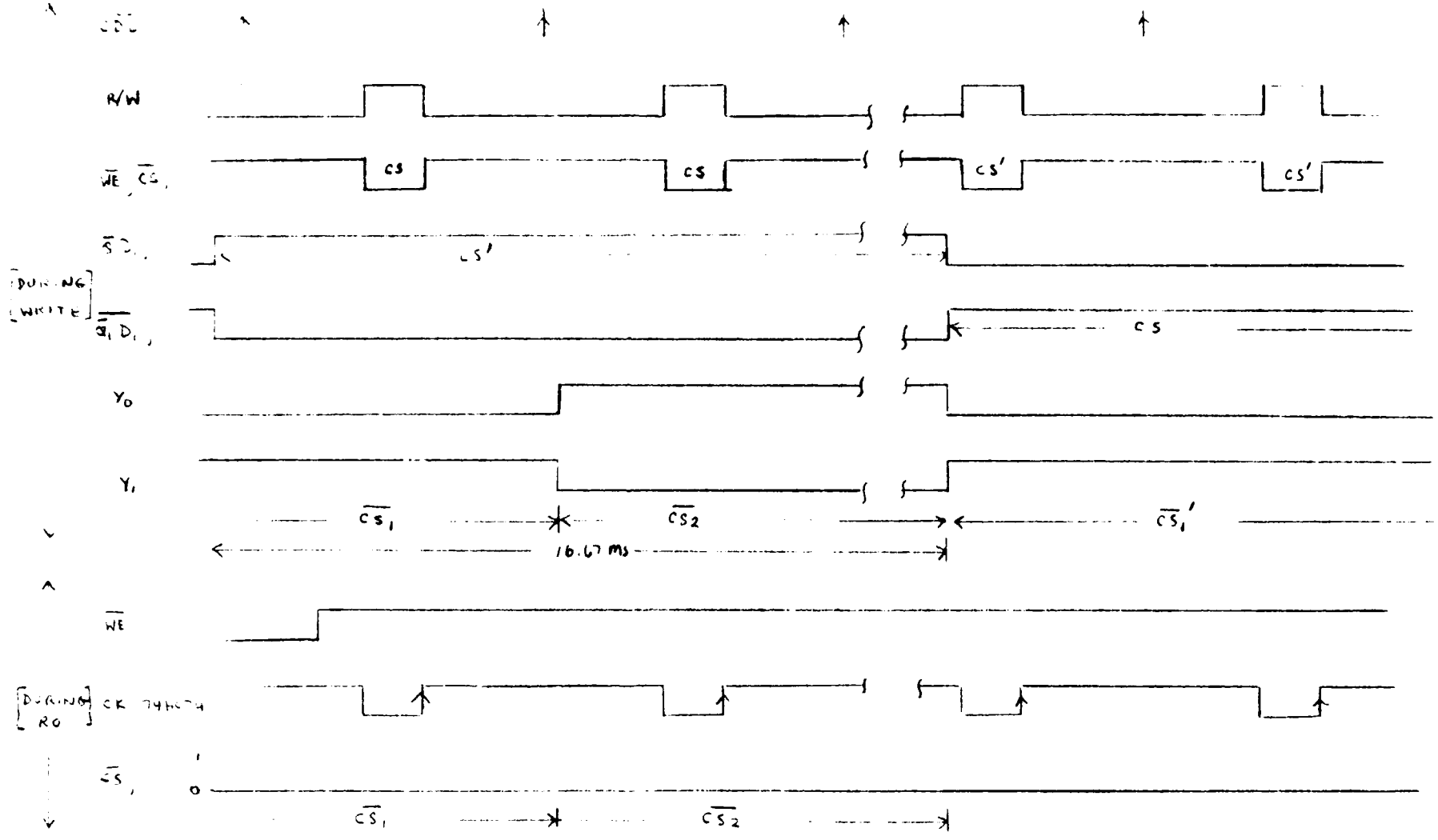


Figure 20 Timing diagram for PCM

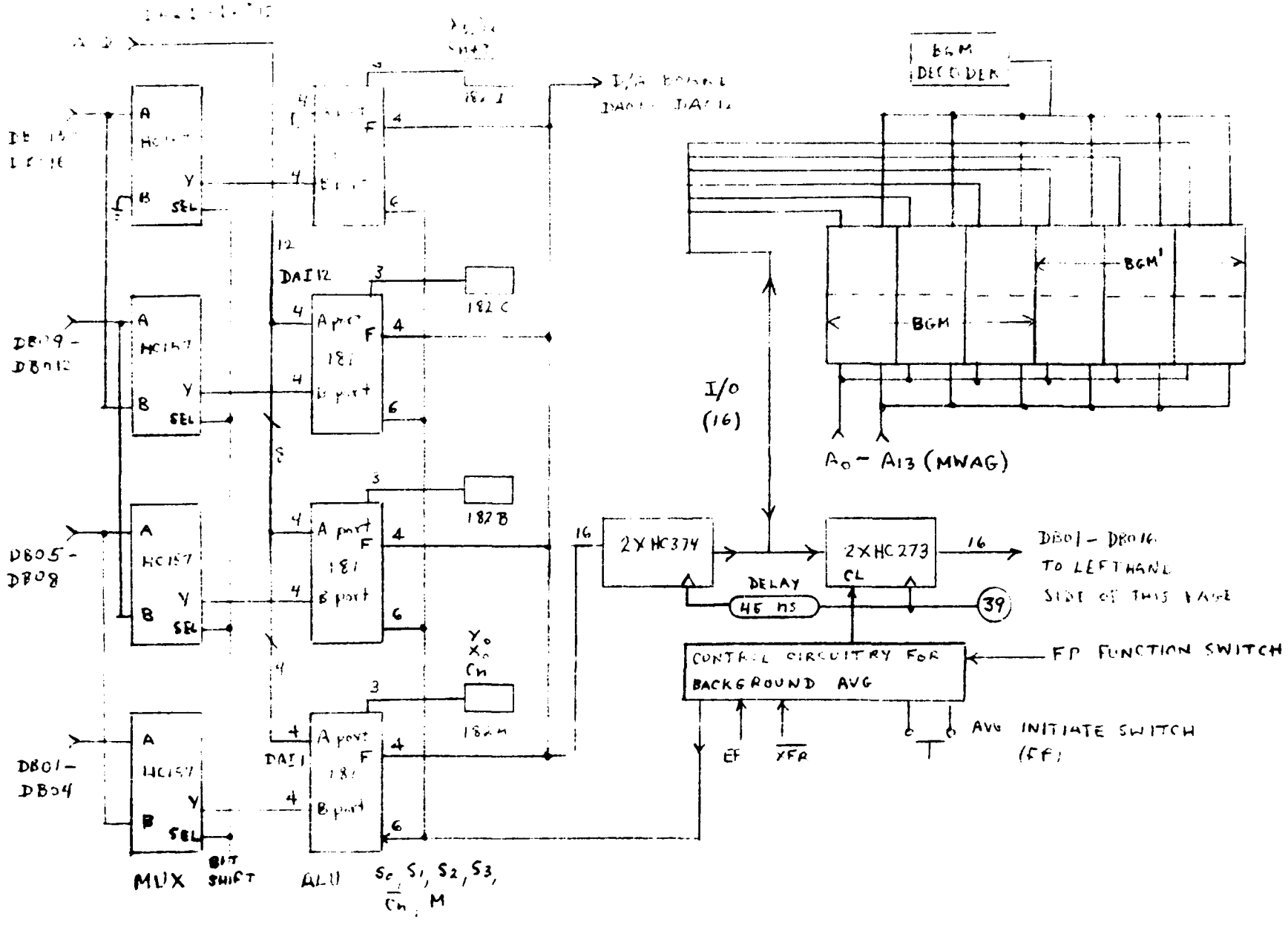


Figure 21 Block diagram of background averaging circuitry and ALU

from the A/D, DAI_1 through DAI_{12}, is the input to the lower three ALU "A" ports. The HC374's are only used to write the BGM with the output of the ALU during the background averaging. Otherwise, the output of the HC374's are maintained in the high impedance state. The 273's are used to readout the BGM to the B inputs via the MUX for all operations.

With the front panel function switch set to AVERAGE, background averaging is initiated by the START AVERAGE pushbutton front panel switch. The momentary closure of this switch results in the bit shift signal going low and remaining low for 16 frames. The low bit shift signal selects the A inputs to the Mux, DBO_1 through DBO_{16}, so that 16 bit operation of the ALU and BGM results. At the end of 16 frames each pixel output has been summed and resides in the BGM. The bit shift signal goes high and now the outputs from the Mux to the ALU "B" port are DBO_4 through DBO_{16}. This shift of 4 bits, division by sixteen, gives the 16 frame average for each Pixel and a return to normal 12 bit operation. Detailed schematics of the BGM, BGM Decoder and BGM latches are shown in Figure 21a.

A schematic of the control circuitry for generating the background average is shown in Figure 22 and the corresponding timing diagram in Figure 23. In Figure 22 the RS FF, 279, and the front panel momentary START AVERAGE switch is used to initiate the background averaging. (Operation of the 279 is indicated in the box at the lower righthand side of Figure 22.) Initially the $\overline{R}_1$ pulse sets Q_1S_1 low and M_1 high thereby gating the 120 for the CK input. Since CK is EF the following "D" type FF_1 will be clocked by the first effective EF pulse as indicated in Figure 23. Q_1 is used for the bit shift signal and since D_1 is low the input CK signal for FF_1 will drive the bit shift signal low at the beginning of the first frame. It will remain low until the next preset pulse PR_1 which occurs at the end of 16 frames. At the same time that Q_1 goes low the output and AND gate 1 rises to activate the two HC193 counters which are used to count the $\overline{XFR}$ pulses at the CU input of $HC193_1$.

The outputs Q_A and Q_B of $HC193_1$ are ANDed and used to clock the "D" type FF_2. Q_1 of FF_2 is set low by $\overline{Y}_1$ of the 120 simultaneously with the activation of the two counters. The first CK pulse to FF_2 will occur only at the end of the first frame when Q_A and Q_B both go high. Since D_1 of FF_2 is held high the rising edge of the first clock pulse will drive Q_1 high and remain high for the remaining frames. This Q_1 output is used for the clear

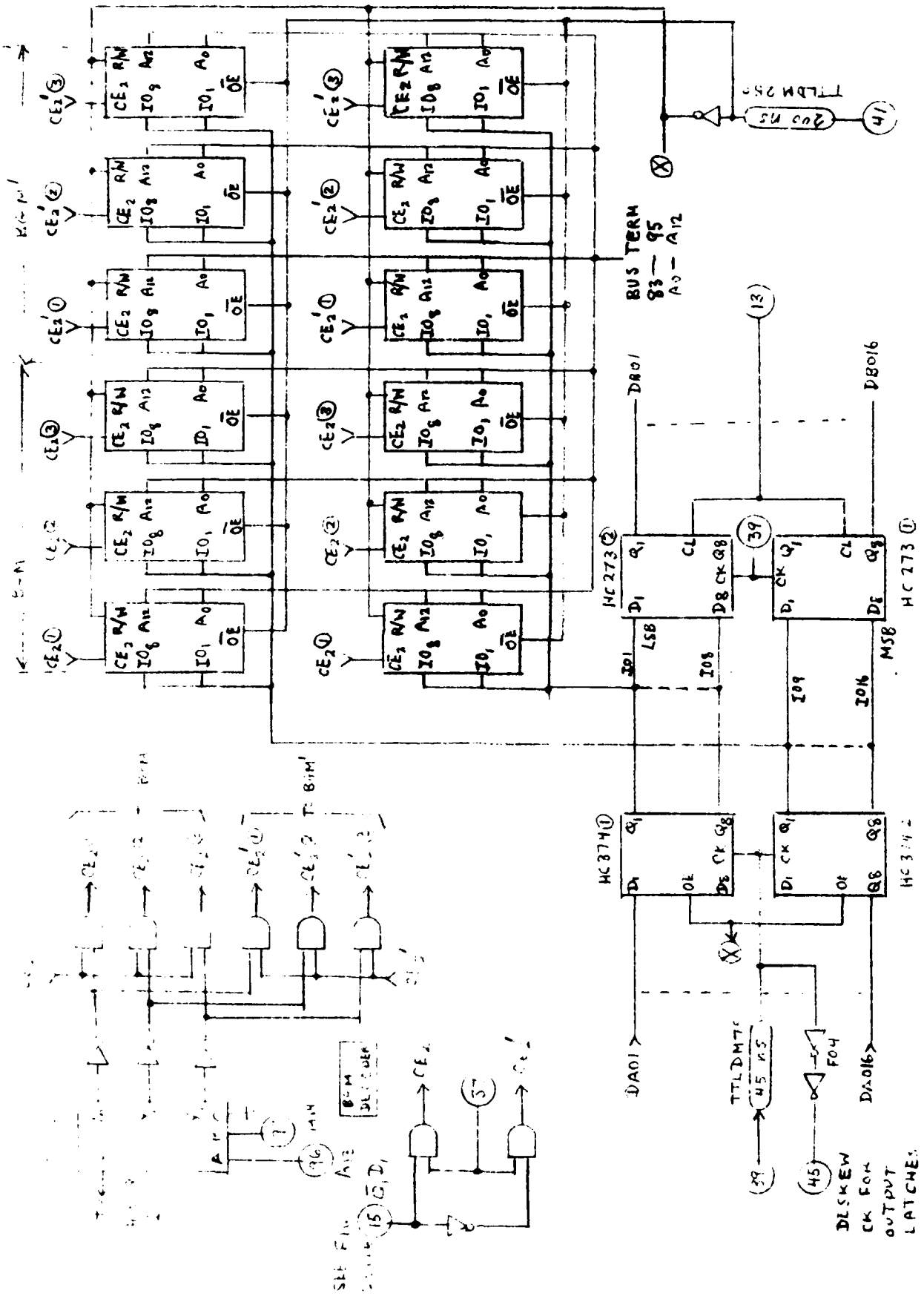
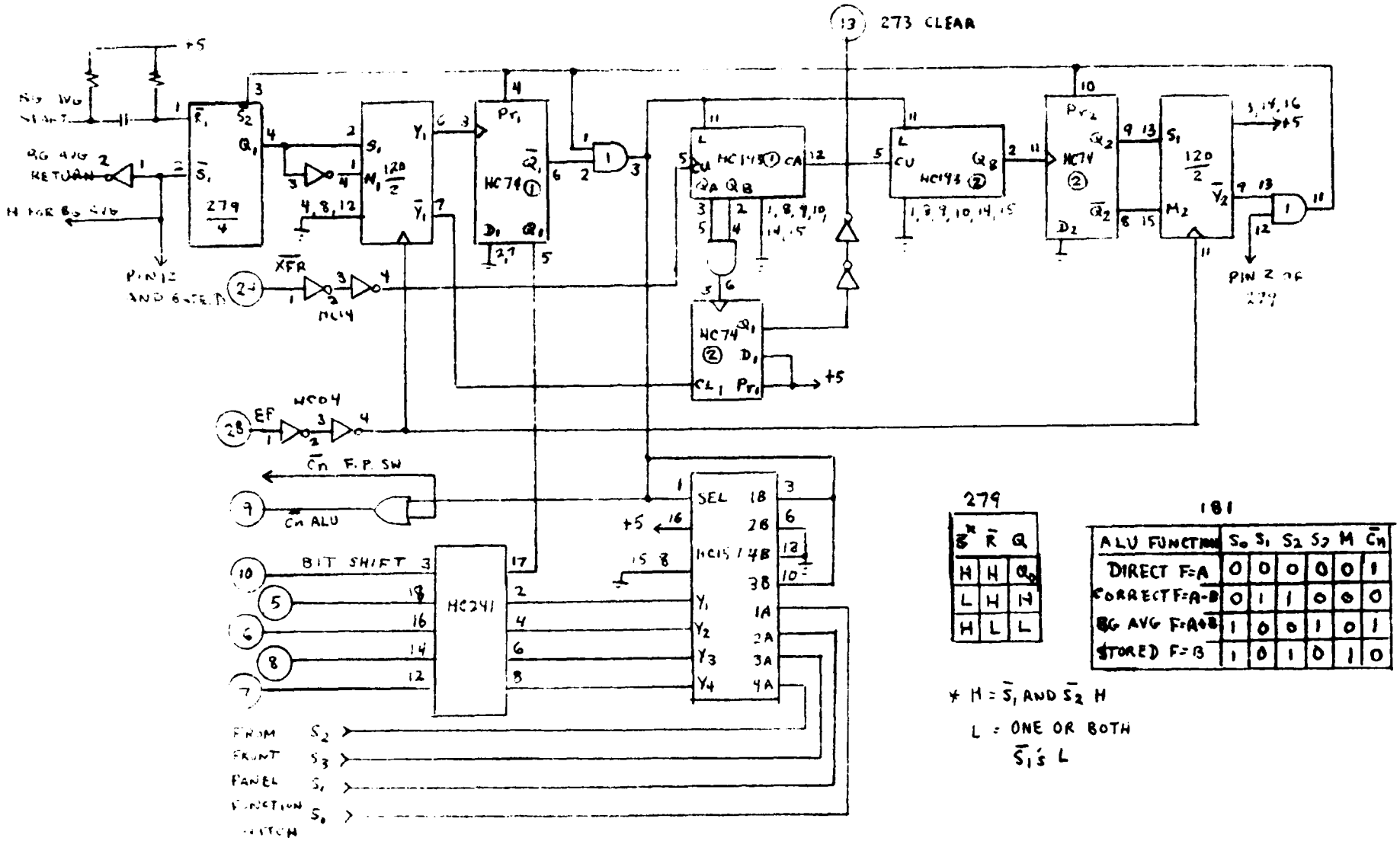


Figure 21a Details of BGM, BGM decoder BGM latches



279

S*	R̄	Q
H	H	Q_0
L	H	H
H	L	L

181

ALU FUNCTION	S_0	S_1	S_2	S_3	M	$\bar{C}_n$
DIRECT F=A	0	0	0	0	0	1
CORRECT F=A-B	0	1	1	0	0	0
BG AVG F=A+B	1	0	0	1	0	1
STORED F=B	1	0	1	0	1	0

* H = $\bar{S}_1$ AND $\bar{S}_2$ H

L = ONE OR BOTH $\bar{S}_1$'s L

Figure 22 Circuitry for background averaging

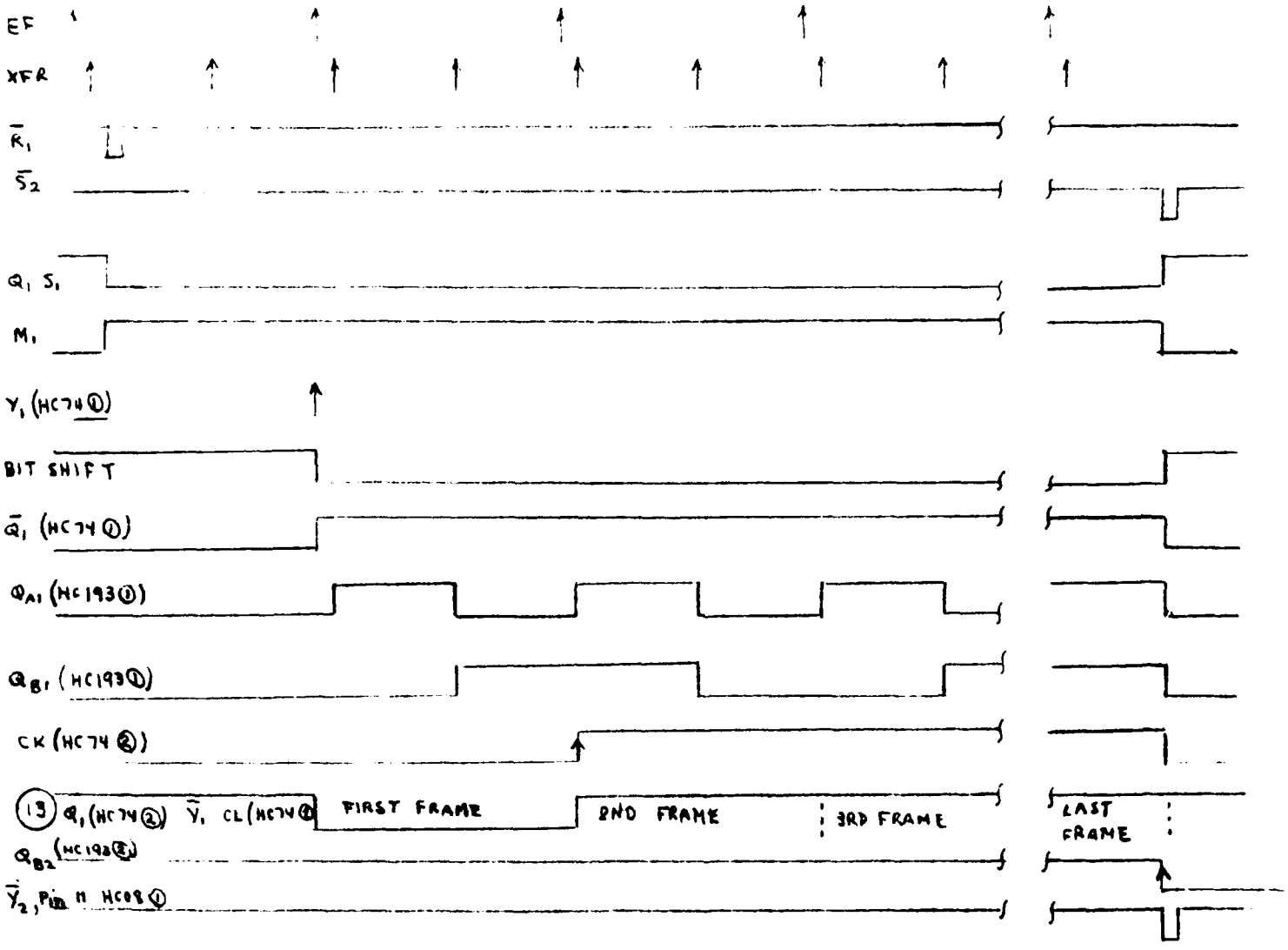


Figure 23 Timing diagram for background averaging circuitry

input to the HC273's. The reason for using Q_1 of FF_2 for the clear pulse for the HC273's will be made evident shortly.

On power up the contents of the BGM are not valid. Consequently, the BGM must be cleared during the first frame. At all times during the background averaging the HC273's are clocked first to allow the BGM output to reach the "B" port of the ALU. During this time the HC374 outputs are in the high impedance state. Next the HC374's are clocked to write the BGM with updated data. Both clocks are operated during each address interval and in the previously stated sequence. See BGM latch circuitry in Figure 21a. However, during the first frame with CL of the HC273's low the inputs to the "B" port of the ALU will be low for each address of the BGM prior to the HC374's being clocked. See righthand side of Figure 24b for HC273 characteristics. As a result at the end of each address interval the BGM will have been written with valid data. At the end of the first frame the BGM will have been fully loaded with valid data. Now CL for the HC273's goes high allowing the CK input to control the HC273's transmission of the BGM contents to the "B" port of the ALU. The contents of the BGM will now represent the sum of all previous valid data. A timing diagram of the operation during background averaging is shown in Figure 24a and for normal operation Figure 24b. See Figures 17 and 18 for the origin of these control signals.

Referring again to Figure 22 and 23 the background averaging operation is terminated after 16 frames by Q_B of $HC192_2$ counter and the 120. Q_B clocks "D" type FF_2 driving S_1 and M_2 of the 120 low and high respectively. The next EF pulse will be inverted at the 120 output Y_2 and ANDed with S_1 of the 279 RS FF. The resultant negative pulse at the output of AND gate will clear the HC 193 counters, preset the "D" type FF_1 and FF_2 and trigger the RS FF 279 back to its original state prior to the start of the averaging operation. Presetting FF_1 drives the bit shift signal high. OE of the HC374's goes high which disables the CK input leaving the HC374's in the high impedance state. See the truth tables and timing diagram for normal operation after background averaging in Figure 24b.

The righthand side of Figure 22 shows the signals required by the ALU and controlled by the front panel function switch. The M signal originates on the front panel and reaches the S100 bus via the interface on the S100-1 board. The remainder reach the S100 bus as indicated in Figure 22.

Under normal operation signals S_0, S_1, S_2 and S_3 reach the bus via the

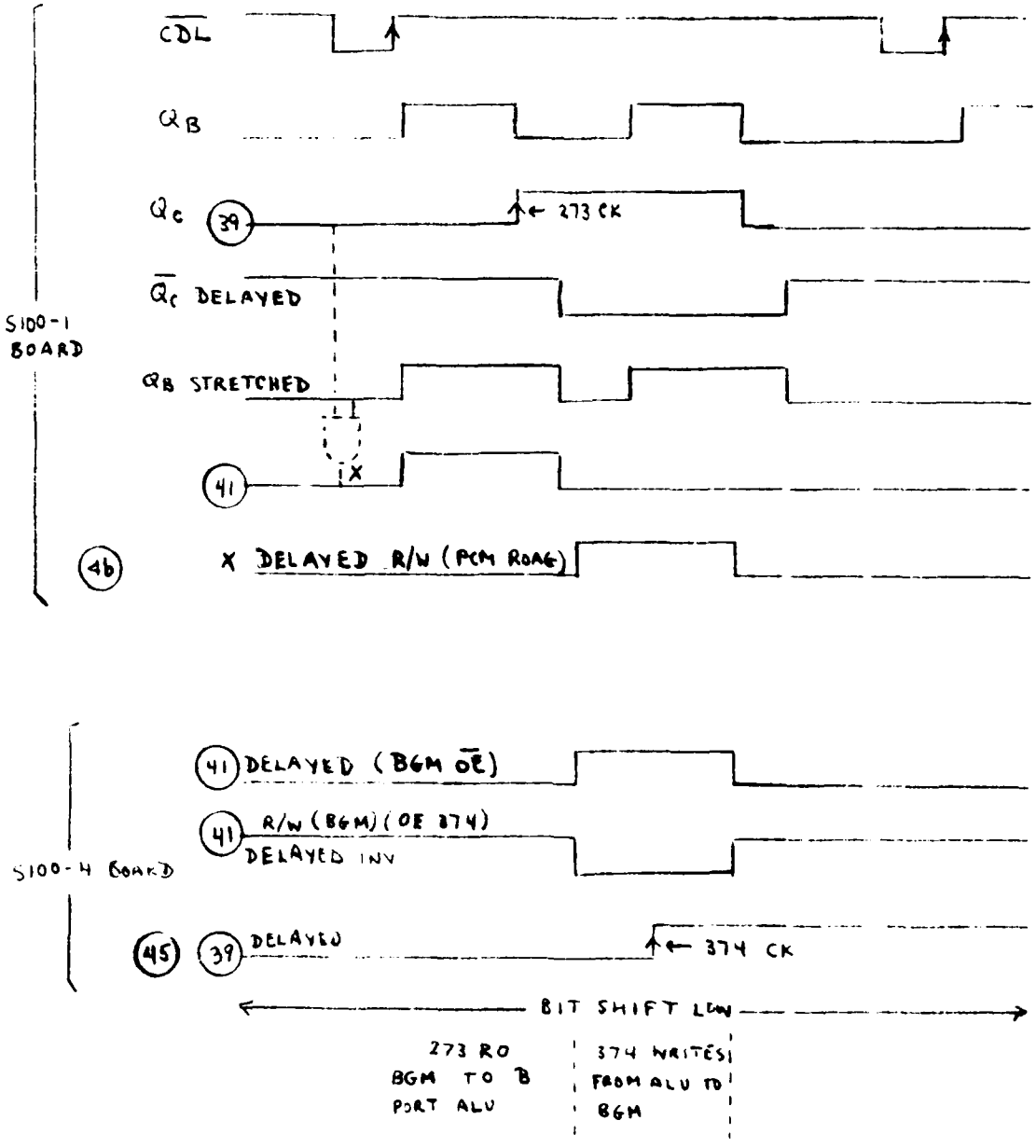
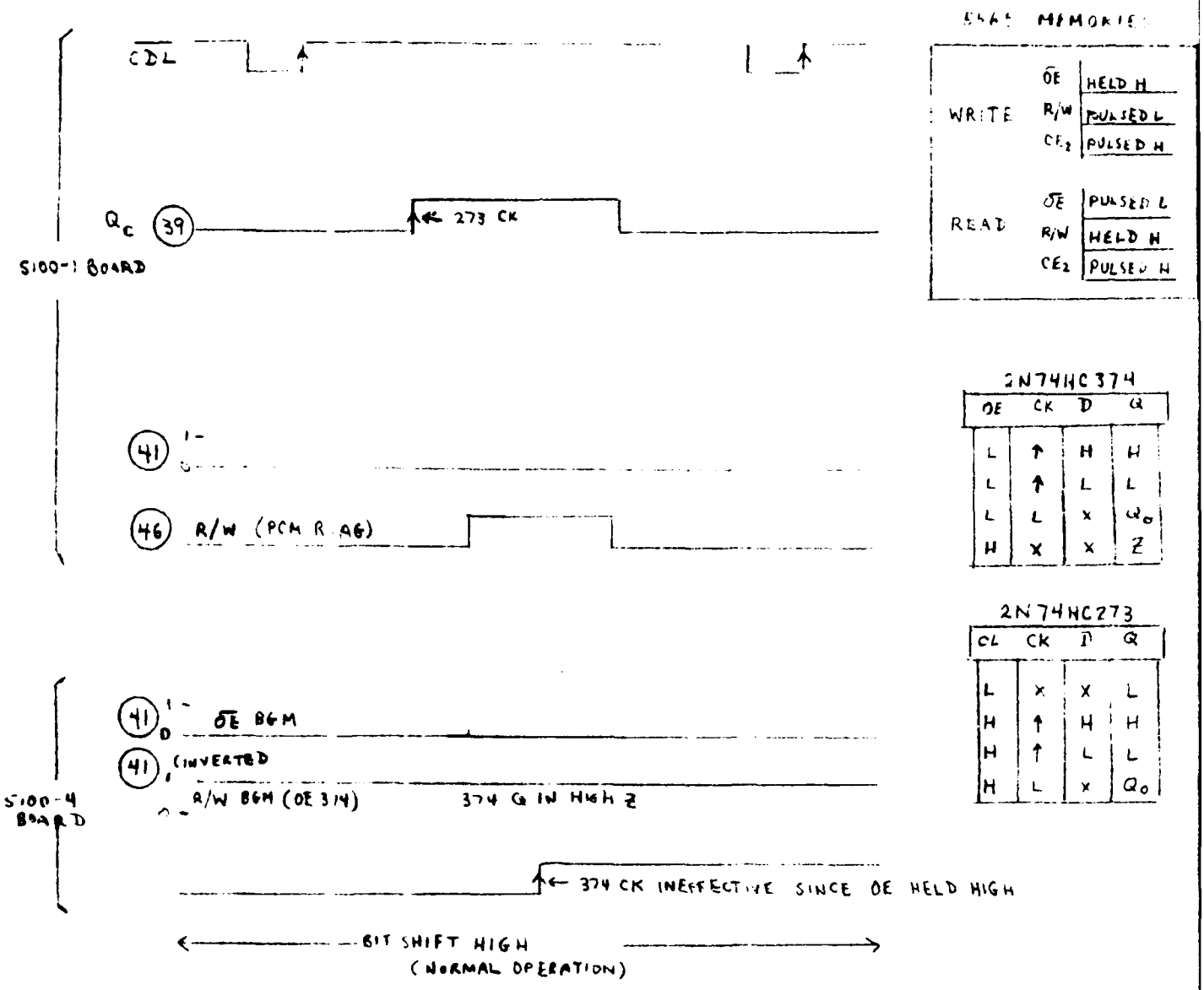


Figure 24a BGM waveforms during averaging



.gure 24b BGM waveforms during normal operation

HC157 mux. Normally the SEL input is low with the A inputs of the mux selected at the Y outputs. Once SEL goes high, during background averaging, the B inputs of the mux are selected yielding the function F = A+B. At the end of the background average the function switch is set to CORRECT yielding the F = A+B function. Now the average background level is subtracted from the incoming data on a pixel by pixel basis.

7. Master Memory Select Circuitry (MMS)

The master memory select pulse (MMS) is used in selecting the FBM's for readout and for being written. In the process of generating MMS an equally important memory select (MS) is obtained and used with the decoders for all memories. Its use has already been discussed for decoding the PCM. MMS and MS circuitry is shown in Figure 25 and the associated timing diagram in Figure 26.

In power up it is essential for the memory select signals to be synchronized with the $\overline{EF}$ pulse. The triple input AND gate in Figure 25 serves to delay the PR_2 input sufficiently such that the first EF pulse initiates the correct relationship for Q_1 and $\overline{Q}_1 D_1$. (In this report MS refers to $\overline{Q}_1 D_1$ or Q_1). Note in Figure 26 the second $\overline{EF}$ pulse has no effect on the timing since Q_1 is already high when it occurs.

This circuit was breadboarded prior to final fabrication and was found to function as desired. On power up the waveforms immediately after t_o in Figure 26 were not observable, however, the relationships illustrated in Figure 26 were observable after all power ups.

8. Vertical Position Circuitry

The vertical position circuitry generates two control signals for the Readout Address Generator (ROAG) as well as controlling the vertical position of the raster. Circuit details are shown in Figure 27 and the associated timing diagram in Figure 28. Note that Figure 28 is not to scale.

Circuit operation is initiated by the negative field drive pulse ($\overline{FD}$) which presets the two "D" type FF's and preloads the HC193 counter according to the settings of the four switches and the R network. FF_1 with $\overline{Q}_1$ tied to

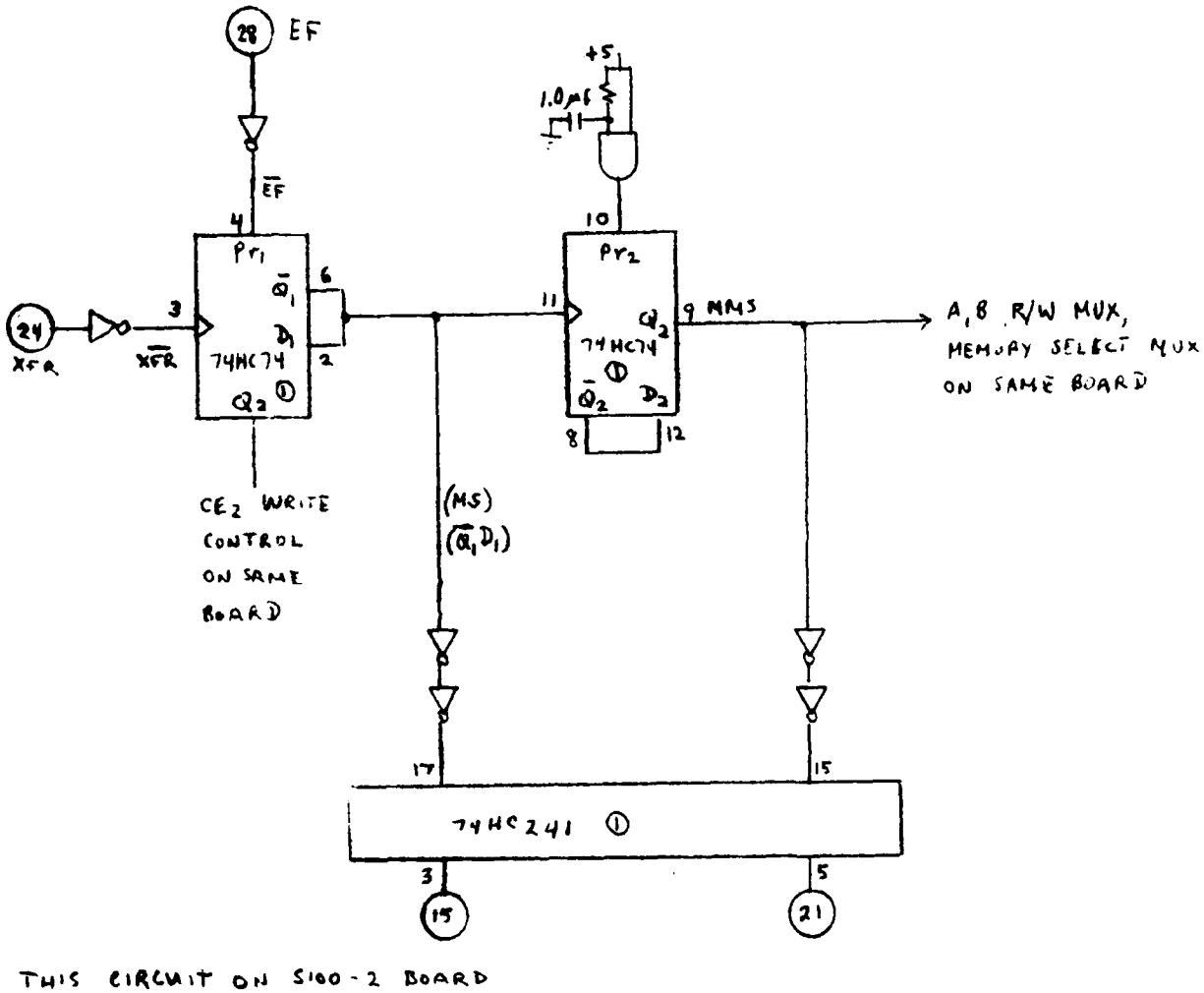


Figure 25 Master memory select circuitry (MS)

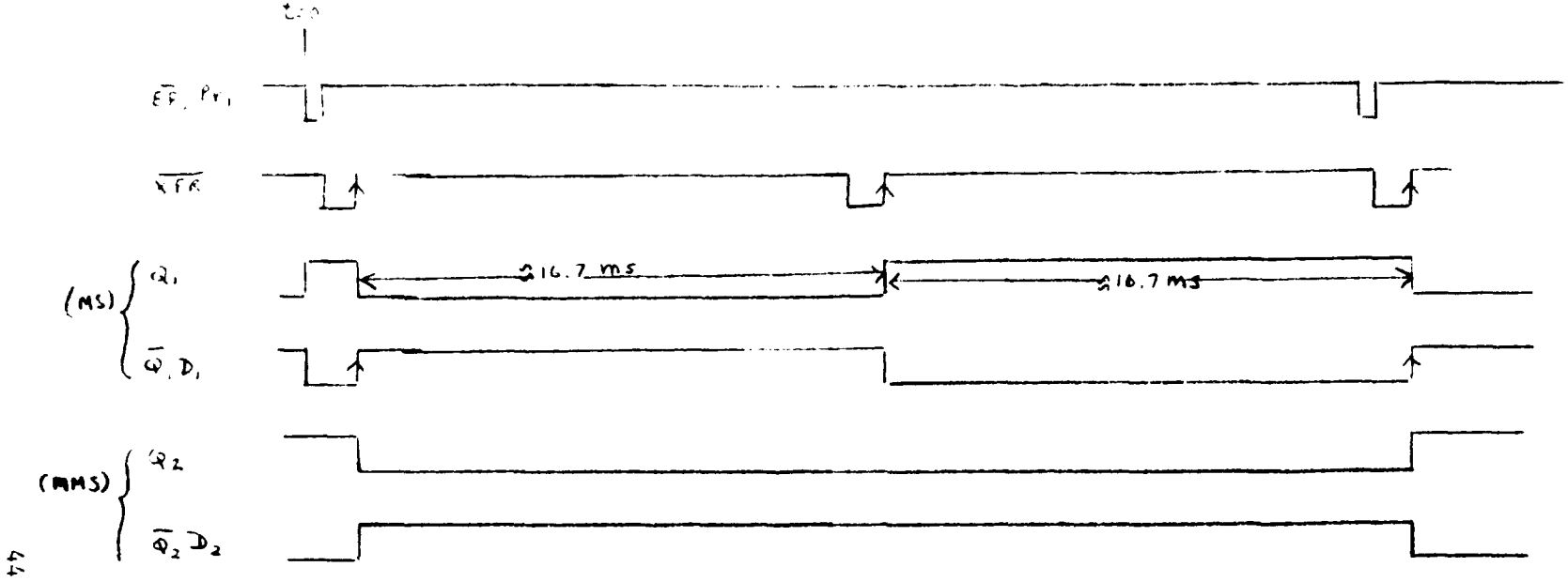


Figure 26 MS timing diagram

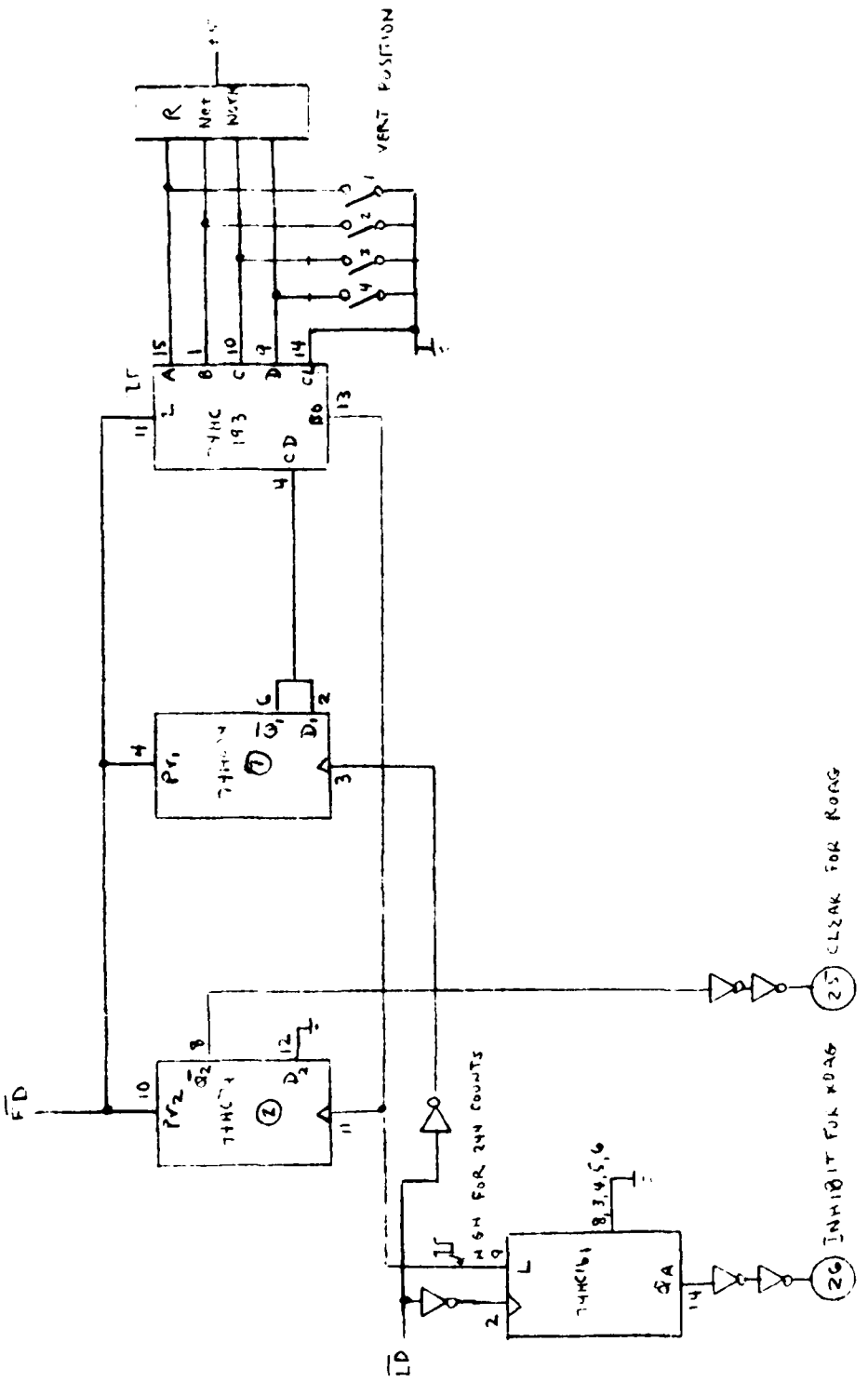


Figure 27 Vertical position circuitry

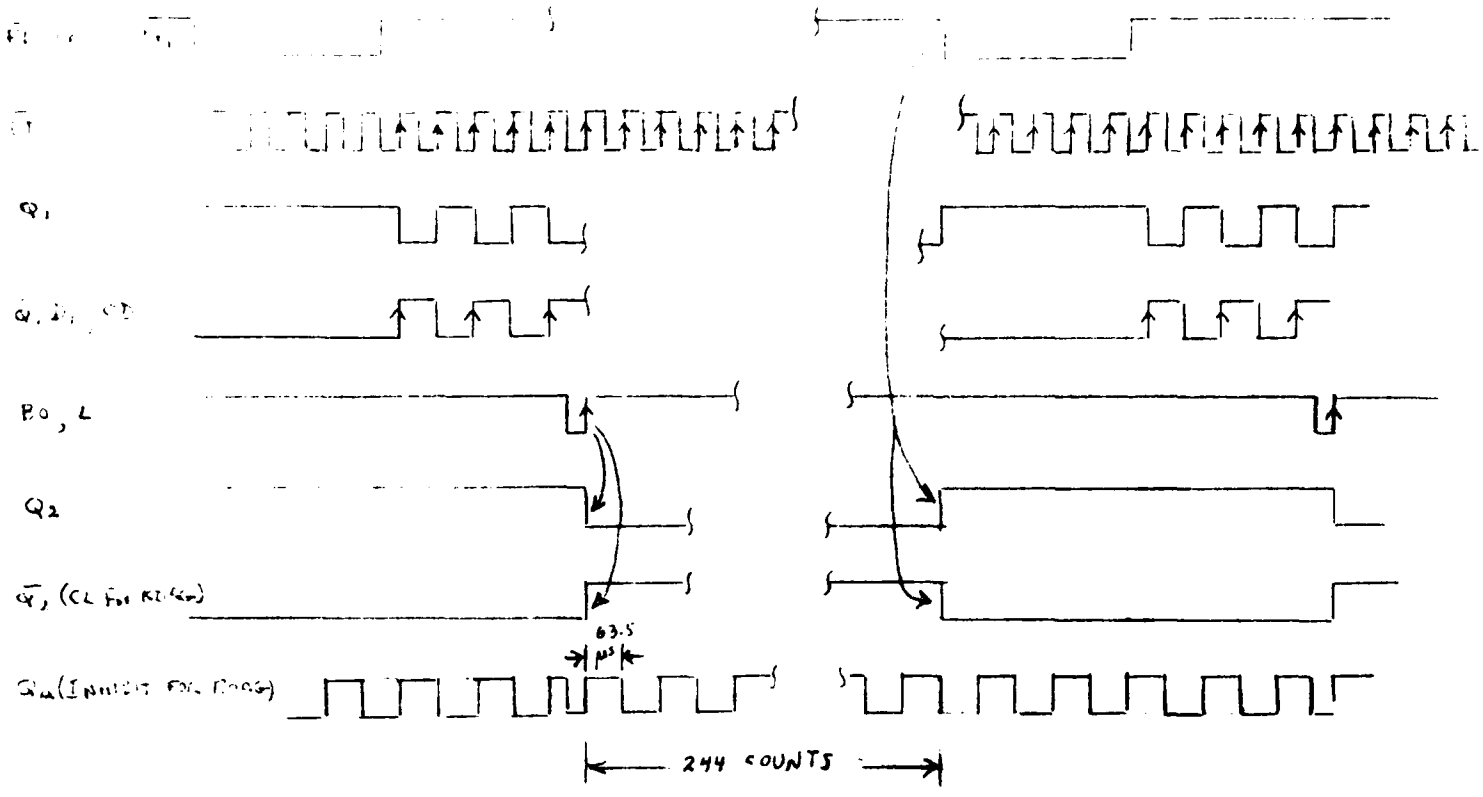


Figure 28 Timing diagram for vertical position circuitry

FF_1 functions as a divide by two circuit with LD being the CK input. Since the count down (CD) input to the HC193 counter is $\overline{Q_1}Q_1$ the counter is incremented on every other $\overline{LD}$ input pulse.

Initially $\overline{Q}_2$ of FF_2 is low as a result of the $\overline{FD}$ pulse. $\overline{Q}_2$ is buffered to the S100 bus and used to clear the HC161 counters of the ROAG. The borrow (BO) pulse from the HC193 counter clocks FF_2 and $\overline{Q}_2$ goes high since Q_2 is inverted. $\overline{Q}_2$ activates the ROAG HC161 counters, and remains high until the next $\overline{FD}$ pulse again drives $\overline{Q}_2$ low.

The BO signal normally high also controls the load ($\overline{L}$) input to the HC161 counter in Figure 27 which is clocked by $\overline{LD}$ pulses. The HC161 counter will be preloaded to 0 by the negative BO pulse and count until the next BO pulse. The interval between BO pulses is 16.67 milliseconds allowing for a maximum of 262.5 lines of $\overline{LD}$ pulses. Output Q_A of the HC161 is a 50% duty cycle square wave with a half period of 63.5 μs. As indicated in Figure 27 J_A is buffered to the S100 bus and used in the inhibit circuitry for the ROAG.

9. Readout Address Generator (ROAG)

A simplified block diagram of the ROAG is shown in Figure 29. The block labelled "MEMORY SELECT" was discussed in Section B7 and the associated waveforms shown in Figure 26. The master memory select output is used for the SEL inputs for Mux A, Mux B and Mux D. When SEL is low the A inputs are selected for the Y outputs.

Mux A and Mux B outputs are for controlling the FBM's. The Mux inputs from the write and readout gates are interconnected between the two Mux's such that SEL determines which FBM is being written or readout. For example, if SEL is low then FBMA and FBMA' will be operated in the write mode, while FBMB and FBMB' will be operated in the readout mode. For SEL high the mode for each FBM will be reversed.

The "ROAD MEMORY CONTROL" circuitry in addition to controlling the "READOUT GATE" also generates the INC signal which increments one or the other of the counters once every 63.5 μs. The sequence of increments is controlled by the "RO COUNTERS INHIBIT" block which is controlled by the J_A input. J_A was discussed in Section B8. Circuit details are shown in Figure 27 and the associated waveforms in Figure 28. When the bottom counters are

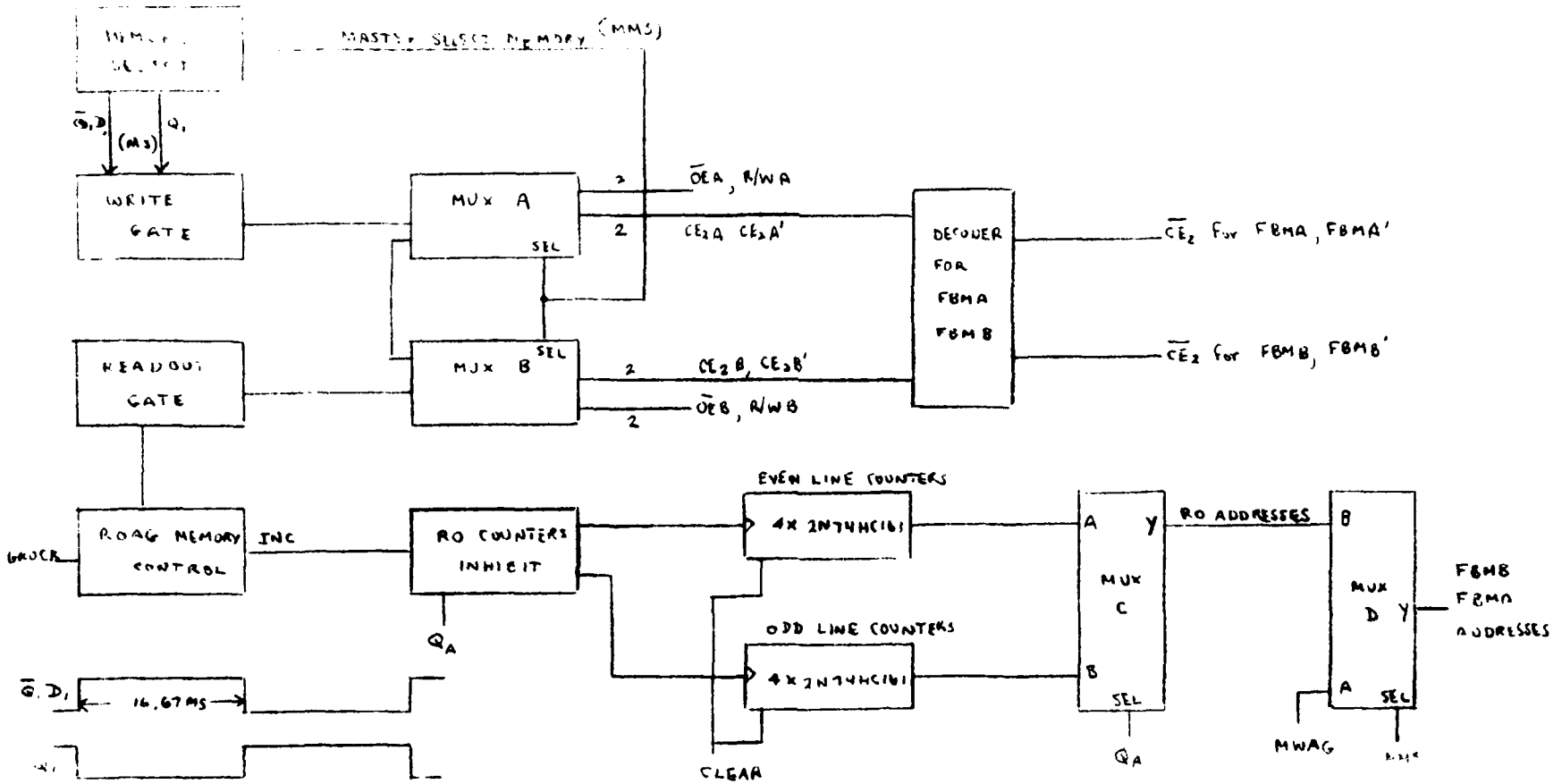


Figure 29 Block diagram of the ROAG

inhibited from counting the upper counters provide 160 RO addresses for the nth even line. When the upper counters are inhibited from counting the lower counters provide 160 RO addresses for the nth odd line.

Q_A is also used for SEL for Mux C. When SEL is low the even line addresses are selected for the Y outputs and the odd line addresses are selected when SEL is high. Consequently, the output of Mux C is synchronized by Q_A to the counters such that the B inputs to Mux D are alternately 160 RO addresses for an even line followed by 160 RO addresses for the corresponding odd line. This process continues for 244 lines until both sets of counters are cleared by the clear pulse shown in Figures 27 and 28.

Mux D uses the master memory select for the SEL input. The A inputs to Mux D are the addresses from the MWAG while the readout addresses are the B inputs. Mux D inputs are interconnected such that when SEL is low the write addresses are sent to FBMA and FBMA', and the readout addresses are connected to FBMB and FBMB'. The reverse is true when SEL is high. (Notice that Mux A and Mux B are selected for the corresponding operating modes.)

A more detailed diagram of the ROAG is shown in Figure 30. CE_2 and CE_2' for writing are obtained from the "WRITE GATE" consisting of two AND gates. One common input for both gates is held high. When SEL is low and $\overline{Q}_1D_1$ is held high CE_2A is maintained high at the output of Mux A. CE_2A' is held low. These inputs to the decoder in conjunction with the inverted outputs of the S139 will sequentially select the FBMA's for writing 122 even lines. This takes 16.67 milliseconds. When $\overline{Q}_1D_1$ goes low for the next 16.67 milliseconds the decoding circuitry provides for sequencing the FBMA' such that 122 odd lines are written. Since SEL is low for 33 milliseconds all 244 lines will be written in one frame interval. During this same frame interval the R/W input to the FBMA's will be pulsed low for each address and CE is held high as required for writing the 5565 memories.

A timing diagram for the decoder when FBMA and FBMA' are being written is shown in Figure 31. A_{13} and A_{14} inputs to the S139 are taken from the output of Mux D when its SEL is low. Y_0, Y_1 and Y_2 are actively low as shown in Figure 31. These are inverted and ANDed with CE_2A and CE_2A'. When CE_2A is held high, outputs CE_2A_0 through CE_2A_2 are obtained sequentially while the other three outputs are held low by CE_2A'. After 14520 addresses the MWA counters are cleared and CE_2A' goes high. Now outputs CE_2A_0

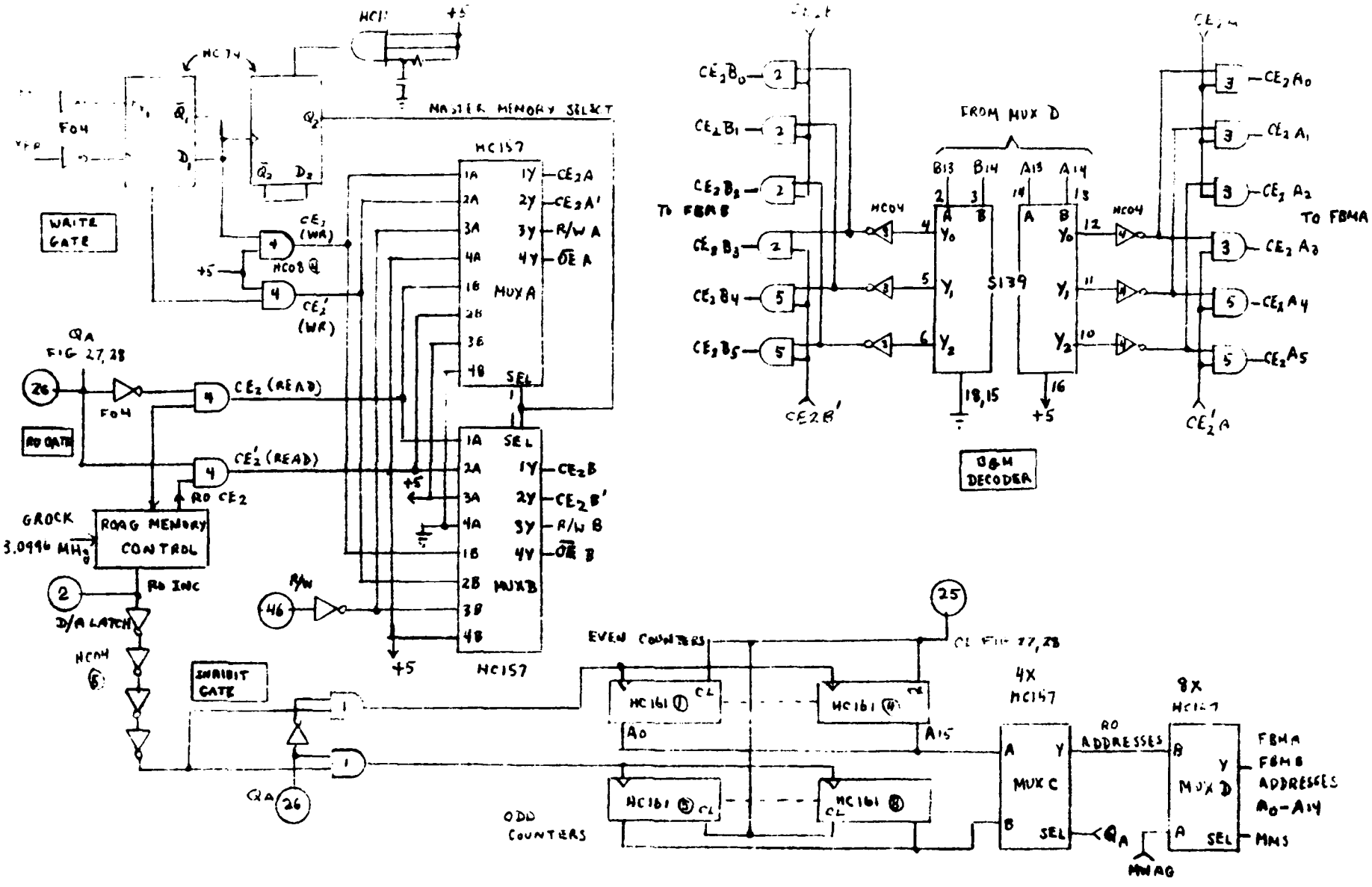


Figure 30 Schematic of the ROAG

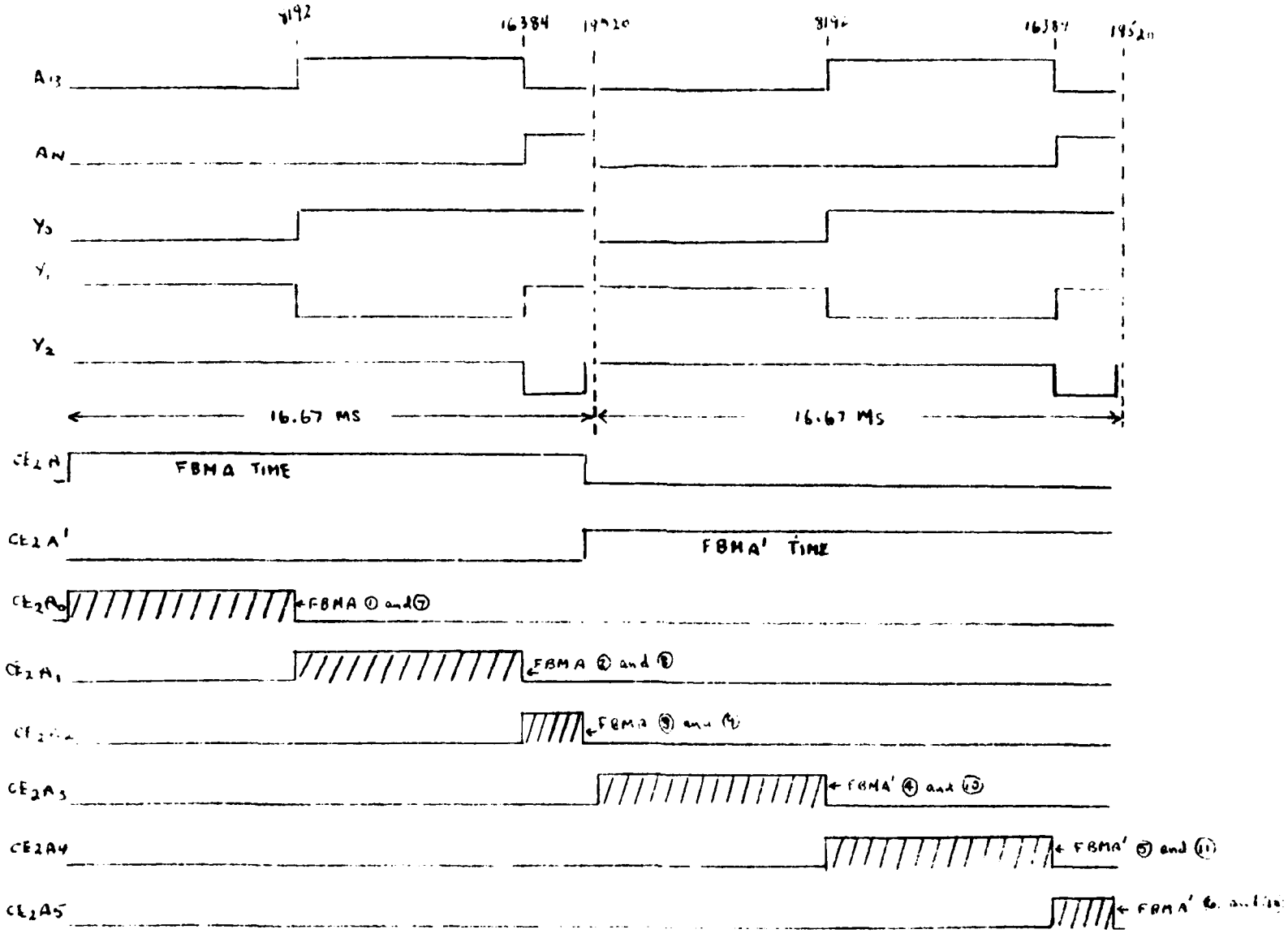


Figure 31 Timing diagram for writing the ROAG

through CE_2A_5 are obtained sequentially while the three previous outputs are held low by CE_2A being low.

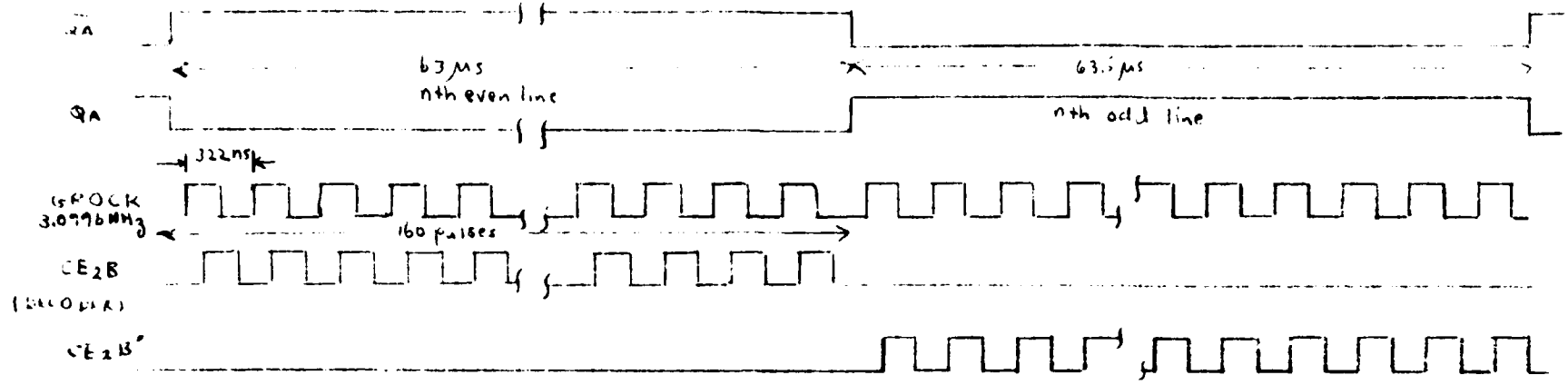
While the A memories are being written once during one frame the B memories are being readout twice. The outputs of the 'RO GATE", CE_2 and CE_2', are synchronized with Q_A. When Q_A is low for 63.5 µs 160 readout CE_2 positive pulses from the "ROAG MEMORY CONTROL" are gated to Mux B and the decoder. The decoder selects the appropriate B memory. Next Q_A goes high for 63.5 µs and 160 readout CE_2' positive pulses are gated to Mux B and the decoder. The decoder selects the corresponding B' memory.

A timing diagram for readout of the nth even and nth odd line from the B memories is shown in Figure 32. This diagram is not to scale. When Q_A is low $\overline{Q_A}$ is high and a pulsed CE_2 (read) will be gated to Mux B input 1A. CE_2B to the decoder will select one of the B memories by means of CE_2B_0 through CE_2B_2. The B' memories will be inactive since CE_2B' is held low.

Now Q_A will be low for 63.5 µs allowing the 160 CE_2B pulses or 160 RO addresses corresponding to say the nth line. When Q_A goes high the CE_2 (read) output will be immobilized and CE_2' (read) will be gated to Mux B input 2A. CE_2B' to the decoder will select the B' memory corresponding to the B memory selected previously by CE_2B and the decoder. Now the B' memory will be selected for 63.5 µs allowing 160 CE_2B' pulses or 160 RO addresses corresponding to the nth odd line.

This ping pong action between the B and B' memories continues until the ROAG counters are cleared after 244 interlaced lines have been readout during 16.67 milliseconds or one TV field. This procedure is repeated, since SEL for Mux A, Mux B and Mux D is held constant for 33 milliseconds, during the next TV field giving 488 lines per TV field.

A schematic of the circuitry represented by the block labelled 'ROAG MEMORY CONTROL" and the associated waveforms is shown in Figure 33. This circuit was designed and breadboarded assuming a 50% duty cycle for the GROCK 3.0996 MHz input. The breadboarded circuit functioned as anticipated. Difficulty was encountered with the "RO GATE" when it was embedded amongst the other circuits on the S100-2 board. The GROCK duty cycle was significantly less than 50%. In the final design the broken line connection corrected part of the difficulty. Other changes involved delaying the INC pulse for the HC161 counters using four HC04 inerters and grounding $\overline{OE}$ to input 4A of Mux B rather than using the pulsed $\overline{OE}$ generated in Figure 33.



ASSUMPTIONS:

1. SEL FOR MUX A, B and D IS LOW
2. R/W B IS HELD HIGH, $\overline{OE}$ B IS HELD LOW
3. DRAWING BASED ON FIGURES 32 and 33

NOTE

DRAWING NOT TO SCALE

Figure 32 Timing diagram for readout of the ROAG

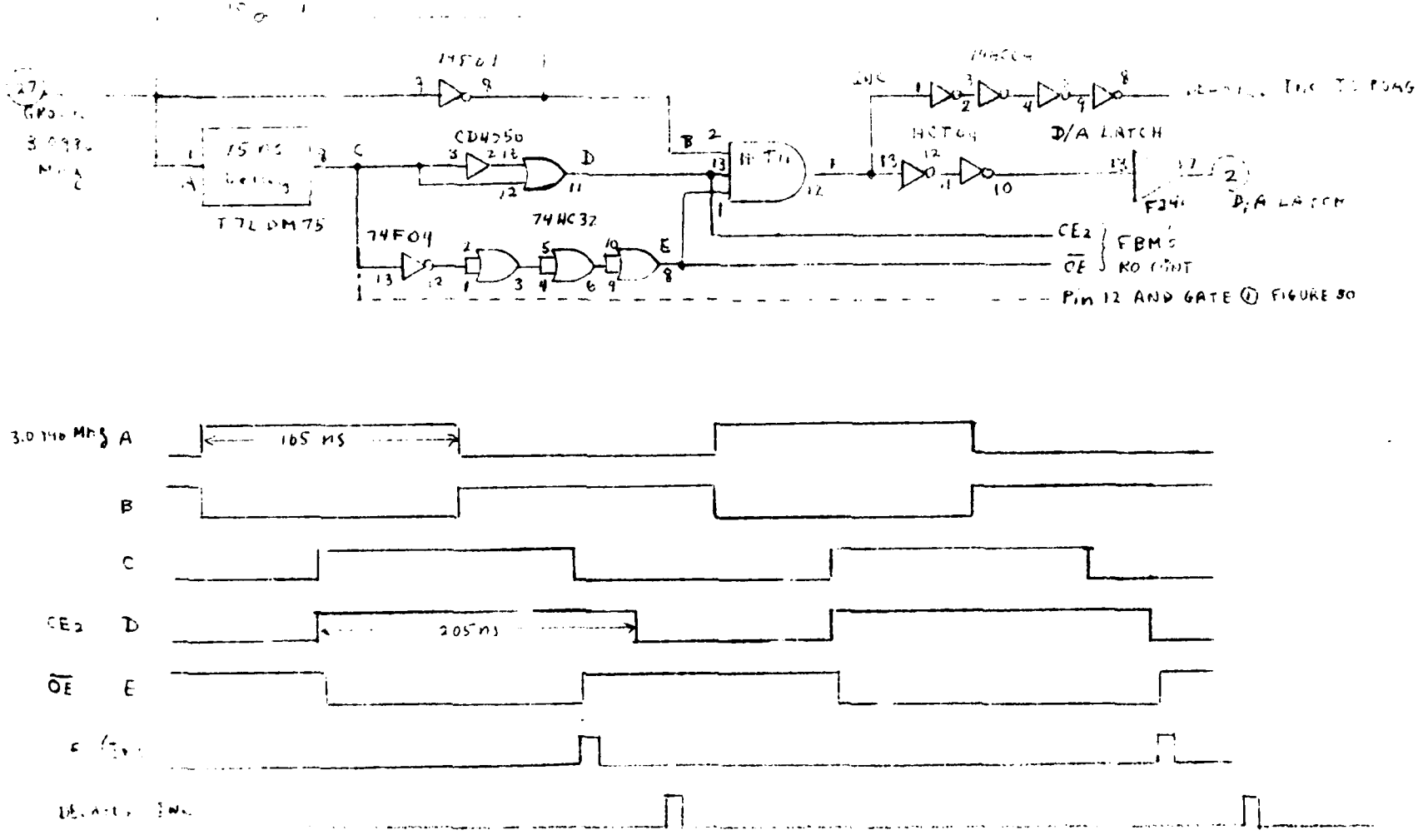


Figure 33 "ROAG MEMORY CONTROL" circuitry and waveforms

A partial schematic of FBMA is shown in Figure 34. FGMB is identical with FBMA. All of the 5565 memory chips are on the same S100-5 board. Twelve bit operation is achieved by pairing chips. For example, memories 1 and 7 are paired and selected by the CE_2A_0 signal from the decoder shown in Figure 30.

Data from the ALU, DAO_1 through DAO_{12}, is bussed to four HC374 latches as indicated in Figure 35. Two latches are used for FBMA and two for FBMB. The outputs of the latches are paralleled with the appropriate I/O ports and the inputs to the mux consisting of three HC157's.

Operation of the circuit of Figure 35 can be explained using Figure 30 and the simplified circuits of Figure 36. In Figure 36A $\overline{OE}$ of the HC374A latch is low while $\overline{OE}$ of the HC374B latch is high. With SEL high the Y outputs of the mux will be the B inputs. Latch HC374B will be in the high impedance state and the contents of the B memory will be read out to the D/A via the mux. Latch HC374A will clock the ALU data to the input of memory A. Reversal of signs for $\overline{OE}$ A, $\overline{OE}$ B and MMS will result in A memory being readout and B memory being written as indicated in Figure 36B.

10. D/A board circuitry

A block diagram of the D/A board circuitry is shown in Figure 37. Processed output data from the ALU at TTL levels is translated to ECL levels by means of four 10124 chips, before getting to the ECL latch. The ECL latch consists of two 10176 chips which are hex ECL "D" type FF's. The outputs of the latch go to the HDS1240E, a 12 bit ECL D/A. Circuit details up to the output of the D/A are shown in Figure 38.

The output of the D/A is buffered by an inverting amplifier, A_1, which is also used for inserting the manual black level input from the front panel control. The inverting amplifier is followed by a switched gain amplifier, A_2, using the Comlinear CLC 220 operational amplifier (OA). Circuit details for this section of the D/A board are shown in Figure 39.

Changing the gain of the CLC 220 OA results in an equivalent offset change at the output. In the original design the CLC 220 was used in the noninverting mode. Difficulty was encountered in controlling the magnitude of the offset variations for different gain settings. This difficulty was

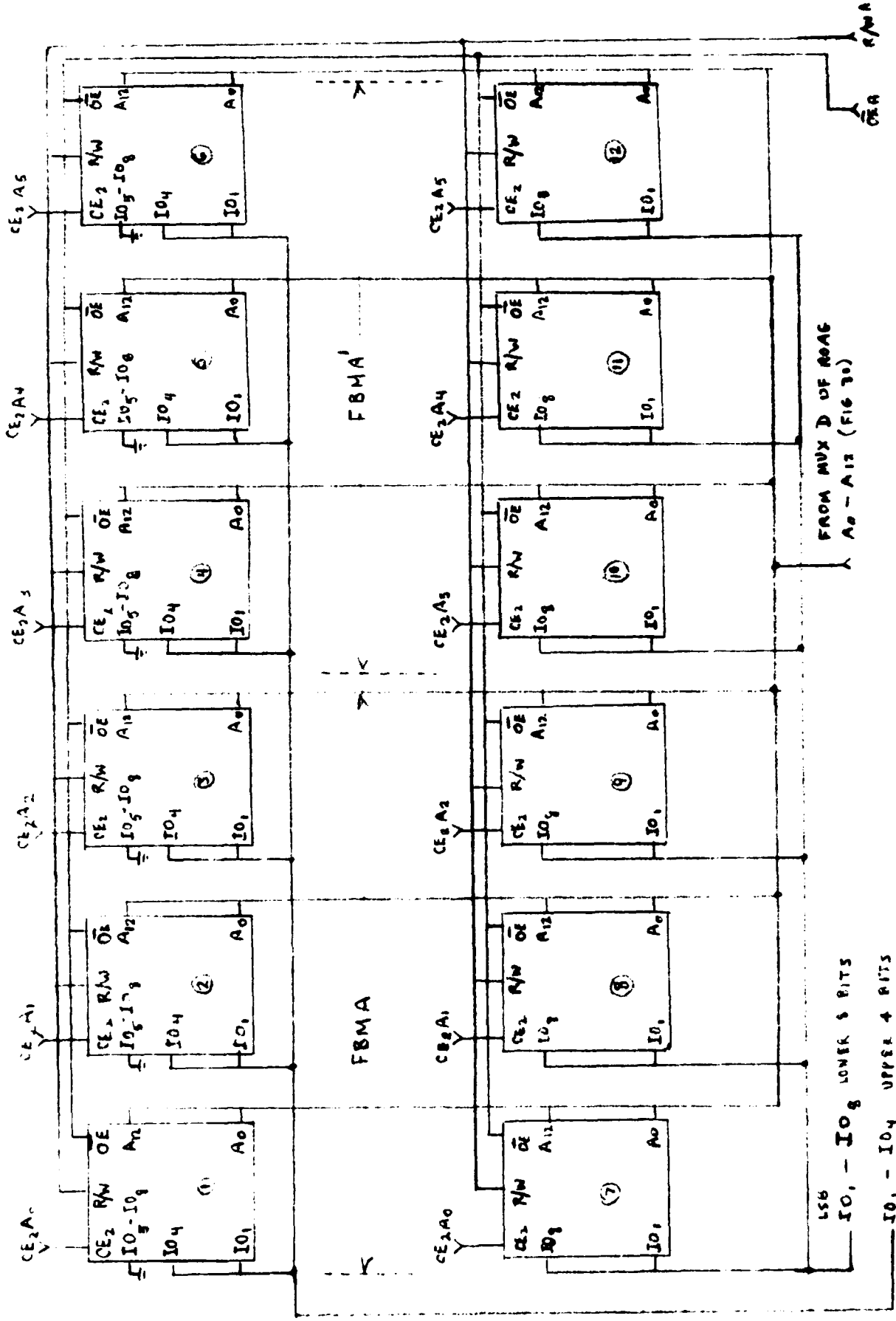


Figure 34 Partial schematic of FBMA

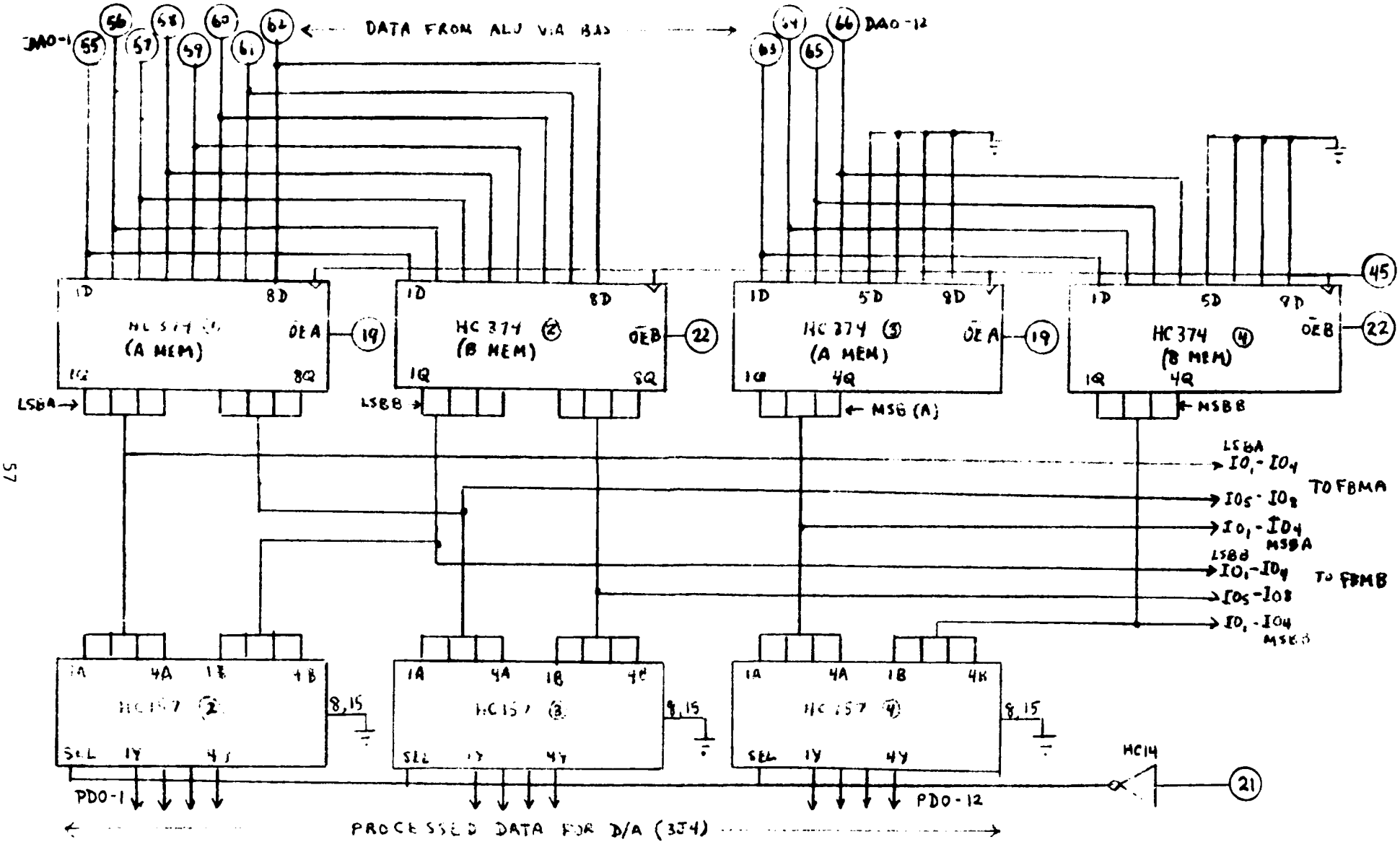


Figure 35 Latch and multiplexed IO data

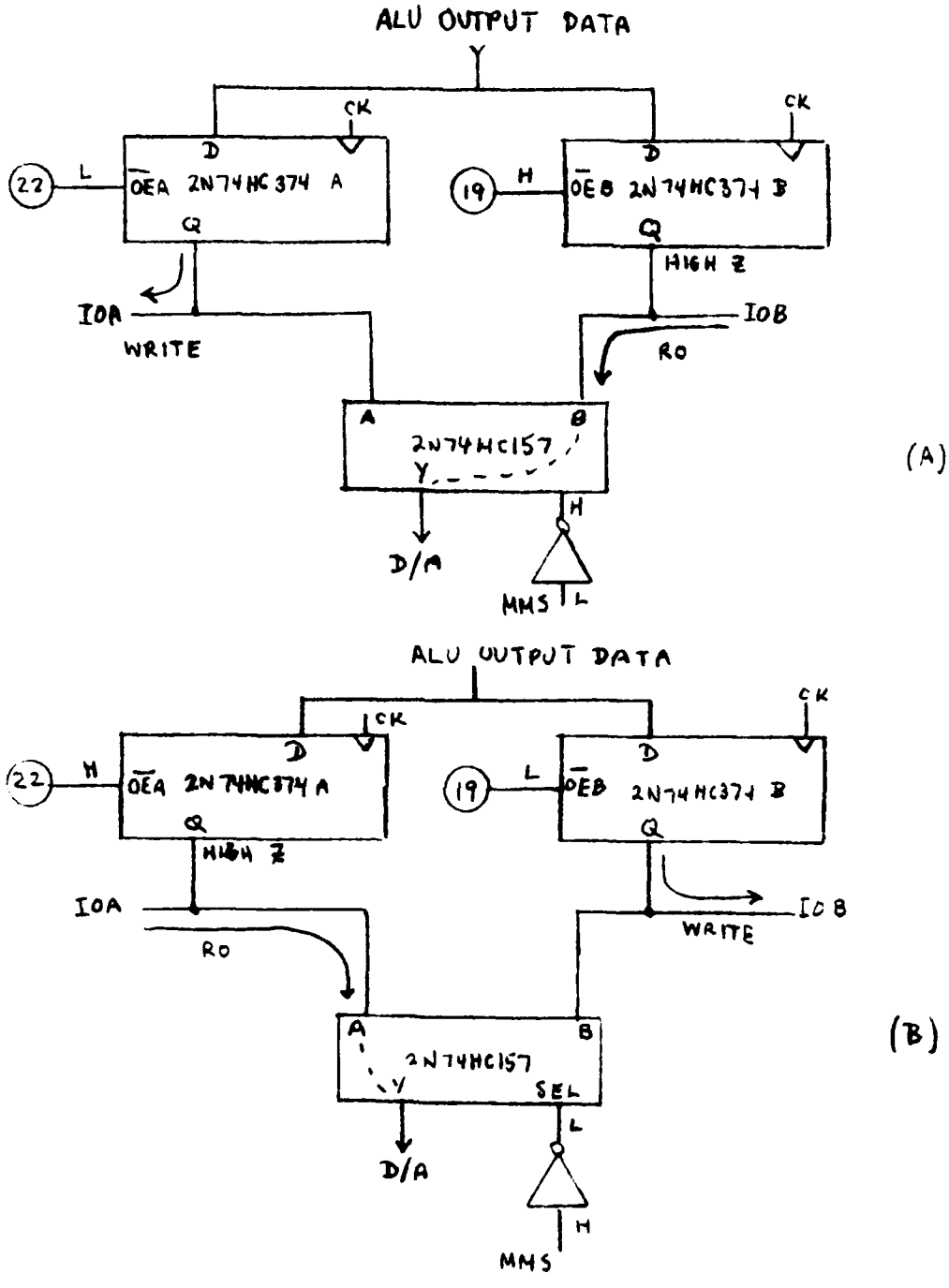


Figure 36 Simplified operation for Figure 35

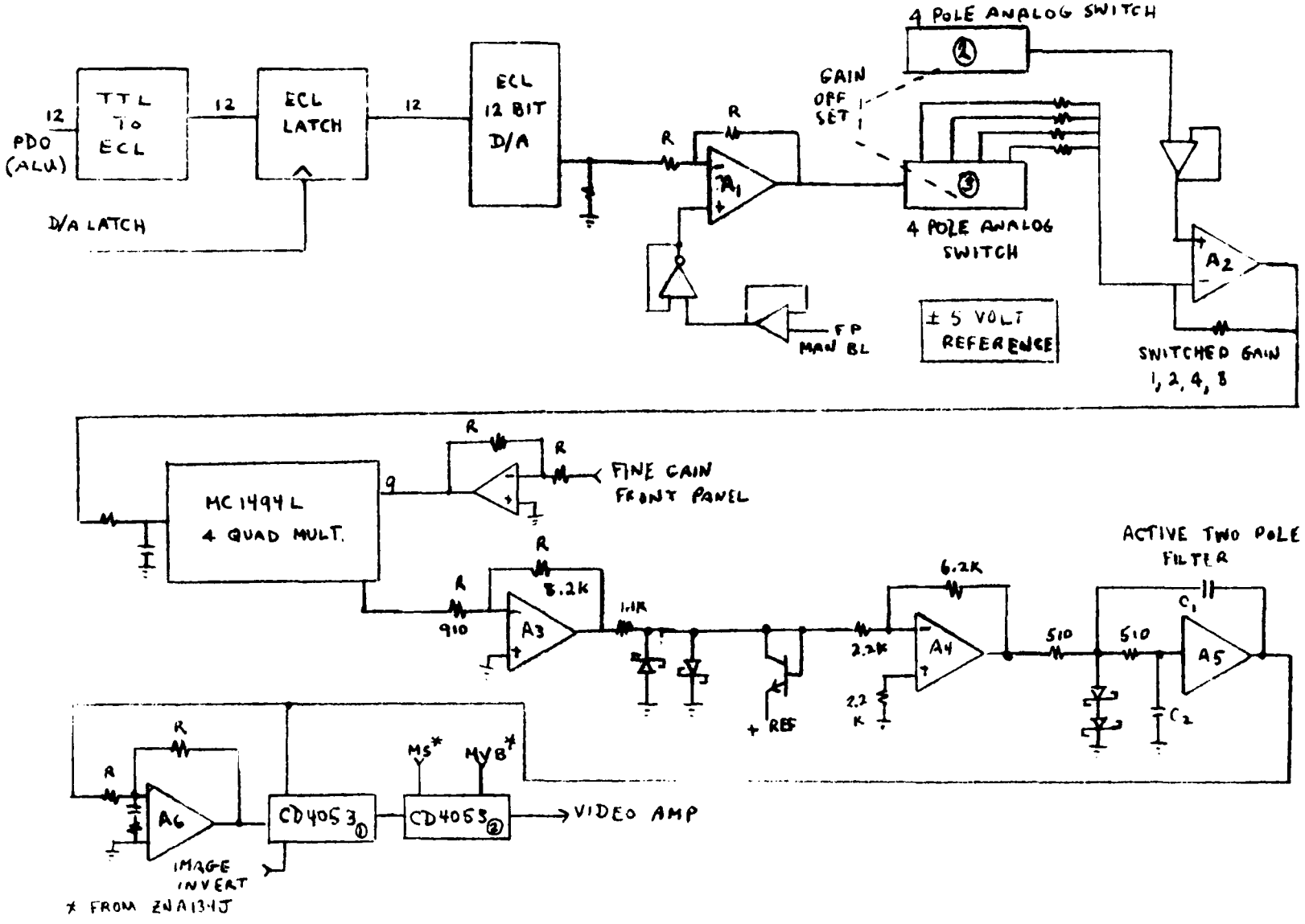


Figure 37 Block diagram of the D/A board

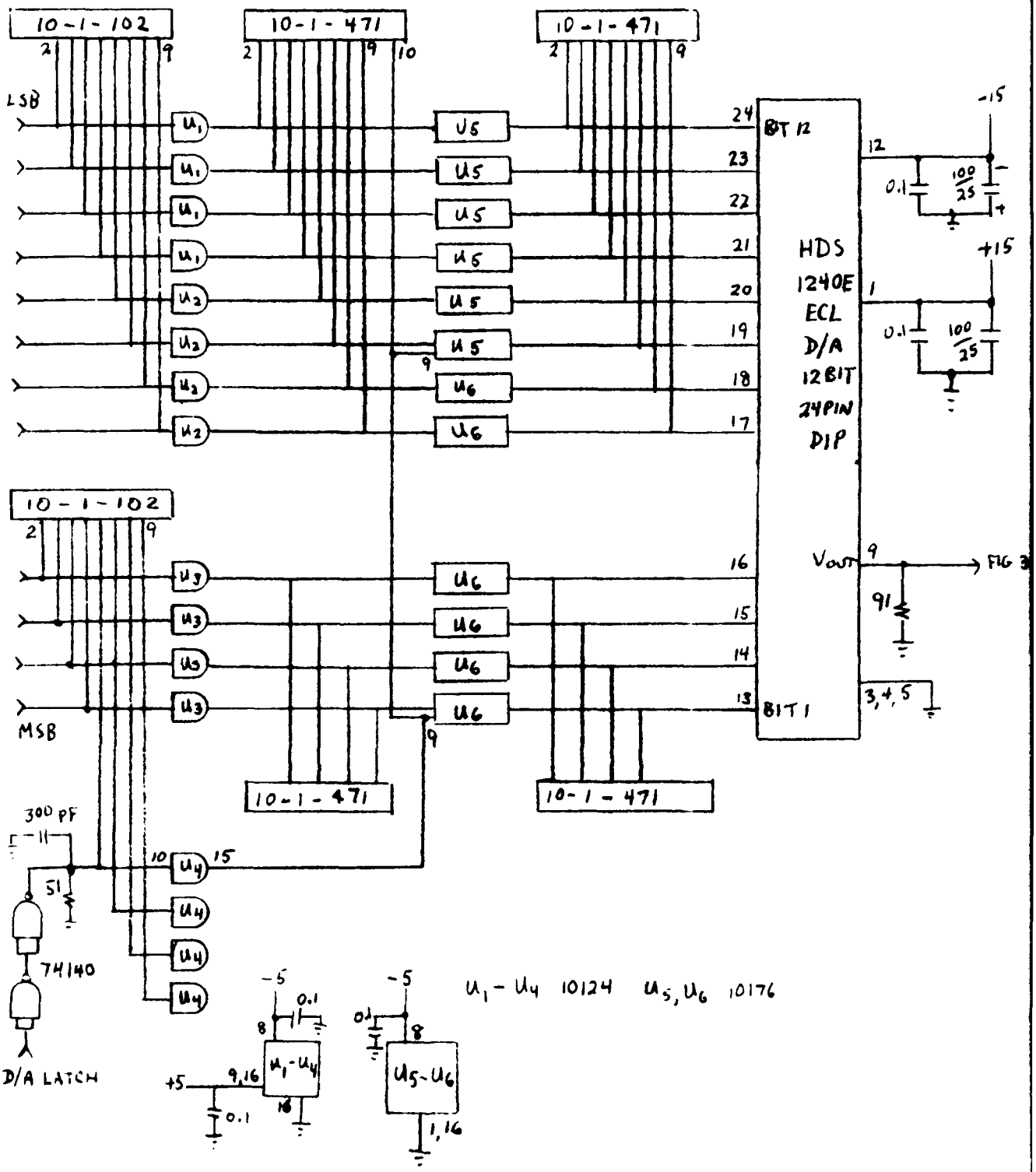


Figure 38 Schematic of the D/A converter circuitry

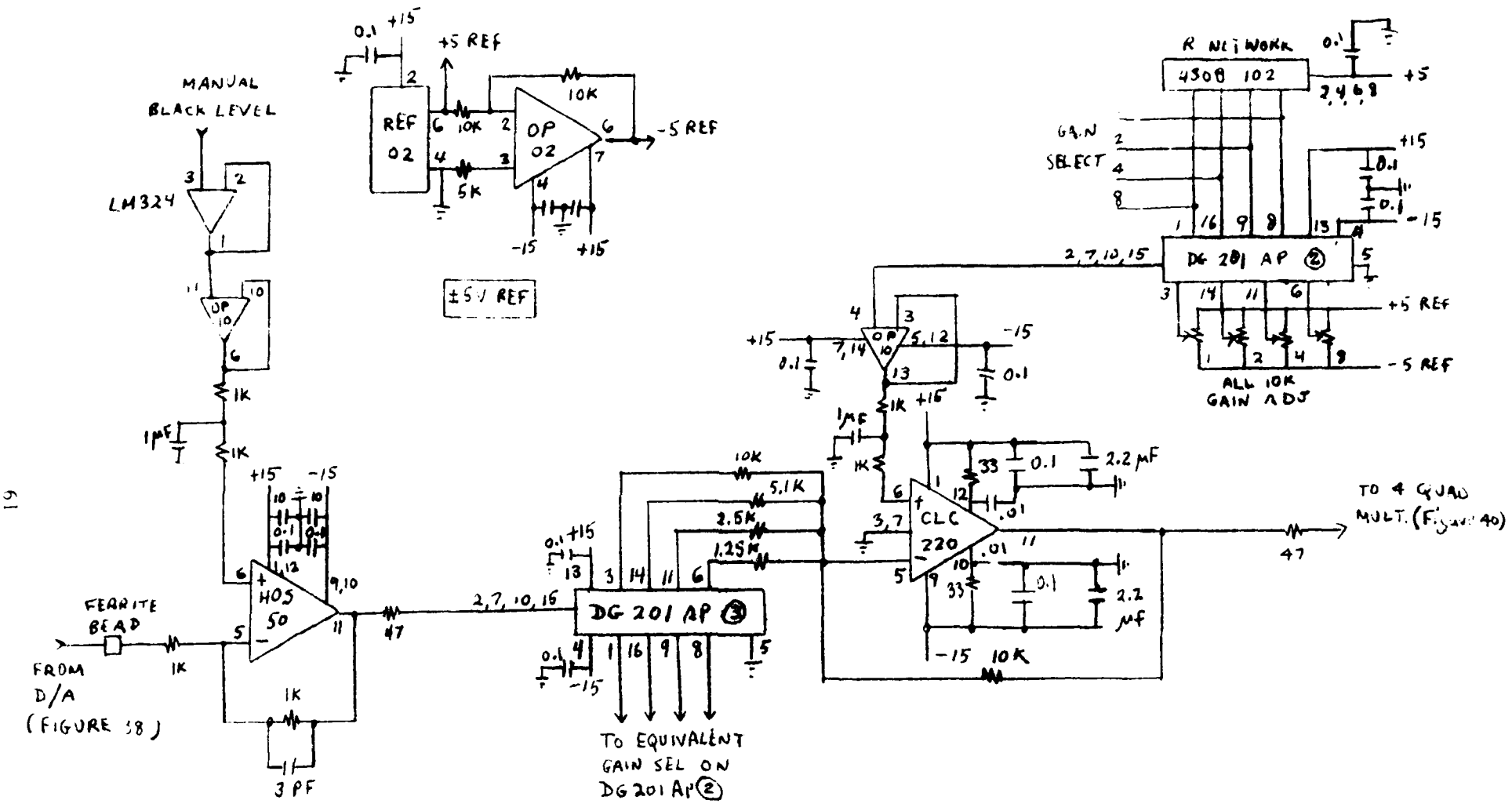


Figure 39 Schematic of the D/A buffer and switched gain amplifier

resolved by using the CLC 220 in the inverting mode where the variations in offset were significantly smaller.

Two four pole analog switches, DG201AP, are used for adjusting the gain and offset simultaneously. A stable offset is obtained using the $\pm$ 5 volt reference supply circuit shown in the upper lefthand corner of Figure 39. The offset output from $DG201AP_2$ is buffered by the unity gain configured OP-10 OA.

In Figure 40 the switched gain stage is followed by a four quadrant multiplier where $V+_y$ is the buffered manual fine gain input from the front panel control. The output of the multiplier is buffered by the CA3100 OA which is followed by the hard limiting SK3100 Schottky diodes and the diode connected NPN soft limiter. This limiting circuitry is used to prevent overdriving the analog transmission gate $CD4053_1$. Additional gain of approximately four is obtained with the HA2520 OA ahead of the two pole active filter.

The two pole active filter in simplified form is shown in Figure 41. It is a low pass Sallen-Key configuration and was designed for a maximally flat magnitude (MFM) response with a half power point of 5 MHz.

The amplifier labelled A in Figure 41 is the BUF-03. The transfer function V_0/V_i is obtained as

$$\frac{Vo}{V_i} = \frac{\dfrac{A}{R_1R_2C_1C_2}}{S^2 + S\left[\dfrac{(1-A)}{R_2C_2} + \dfrac{1}{(R_1\ R_2)C_1}\right] + 1/(R_1R_2C_1C_2)}$$

When A = 1, (A = 0.997 typically for the BUF-03) and $R_1 = R_2 = R_1$

$$\frac{V_o}{V_i} = \frac{\dfrac{1}{R^2C_1C_2}}{S^2 + \dfrac{S2}{RC_1} + \dfrac{1}{R^2C^1C^2}}$$

For an MFM function

$$\sqrt{2}B = 2/RC_1 \text{ and } B^2 = 1/(R^2C_1C_2).$$

Therefore

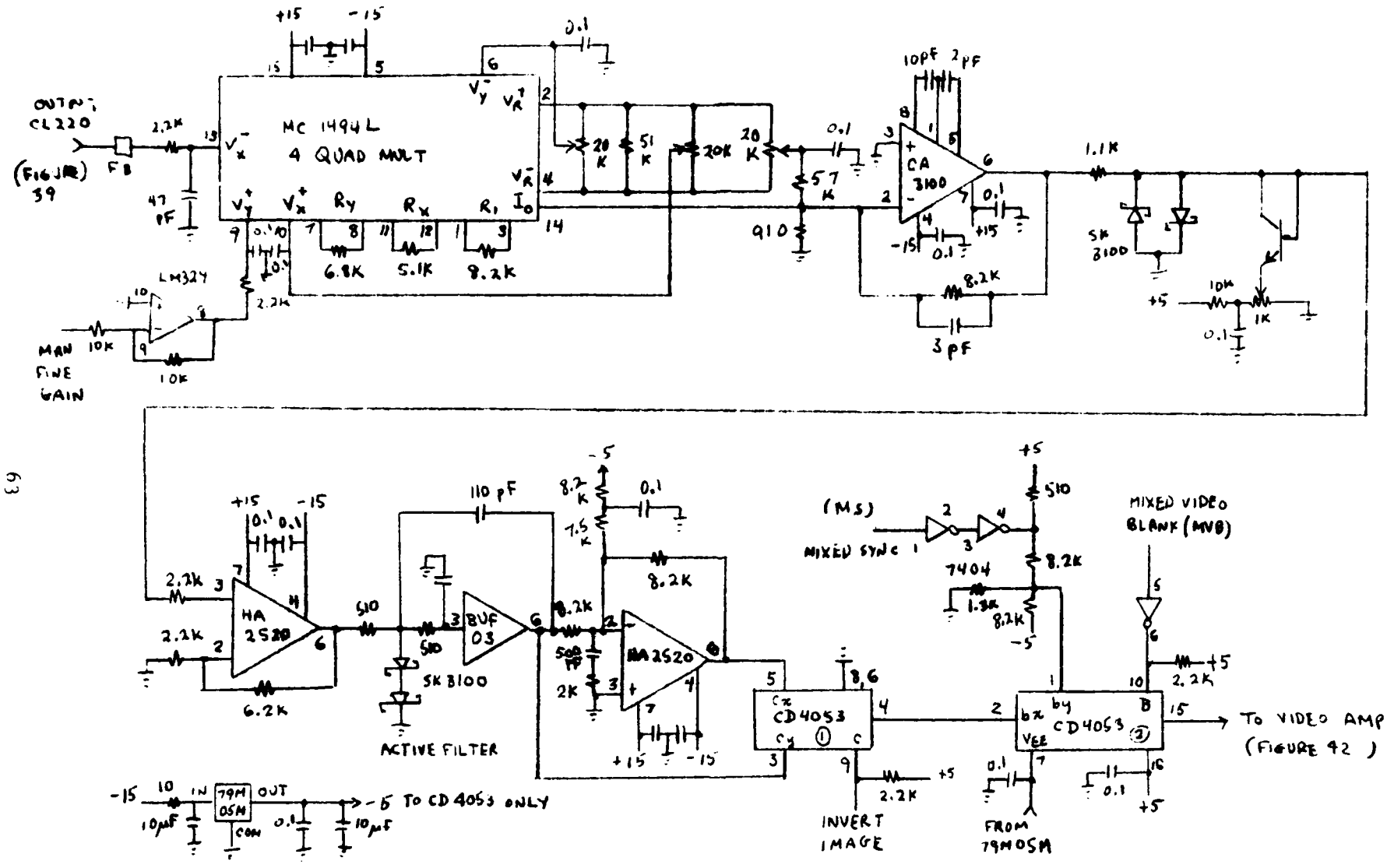


Figure 40 Schematic of D/A board gain stages and active filter

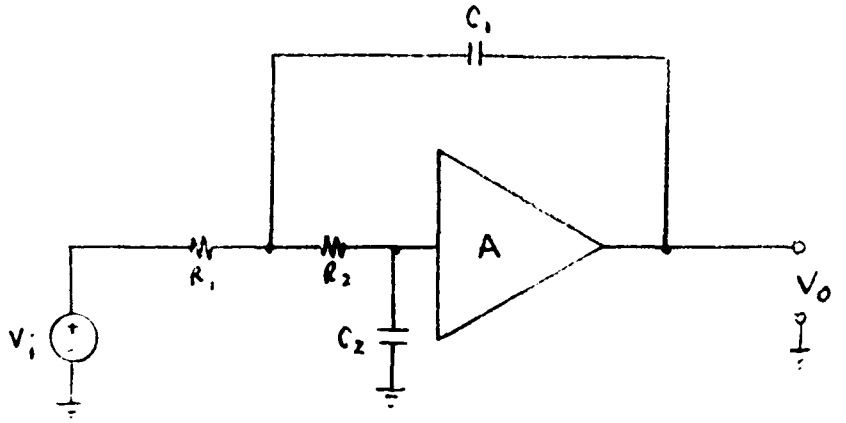


Figure 41 Simplified active filter circuit

$C_1 = \sqrt{2}/RB$ and $C_2 = 1/(\sqrt{2}\ RB)$

and

$C_1/C_2 = 2$ or $C_1 = 2C_2$.

For B = 2π x 5x10⁶ and $R_1 = R_2 = 510$

$C_2 = 44$ pF and $C_1 = 88$ pF.

Originally C_1 and C_2 were chosen as 50 and 110 pF respectively. In fine tuning the overall camera system C_2 was changed to 300 pF without any change in C_1. This value for C_2 does not give an MFM response, however, the reduced bandwidth does result in less noise without degrading the video output.

The CD4053 is a triple two channel transmission gate with inhibit. c_x input is the inverted analog signal from the active filter. c_y input is the direct output from the active filter. When the digital control input "C" is a logic "1" the switch output at pin 4 will be c_y. If "C" is a logic "0" the output is c_x. The "INVERT IMAGE" front panel switch controls "C" for either output.

The second CD4053 output is controlled by the mixed video blank (MVB) from the ZNA134J since it controls the switch logic control "B". When "B" is high the output is b_y or the mixed sync (MS) from the ZNA134J. With "B" low the output at pin 15 is b_x or the analog signal from $CD4053_1$. The composite video at the output of $CD4053_2$ is coupled to the video amplifier shown in Figure 42.

11. Power requirements

In the initial design of this camera the experience gained from the design and operation of the 64x128 camera was utilized as much as possible. It was decided to investigate the possibility of using a single transformer with multiple windings rather than using individual regulated supplies for each voltage. At this time thought was also given to going to switching supplies to reduce weight and size, however, the fear of excessive noise from such supplies deterred this approach.

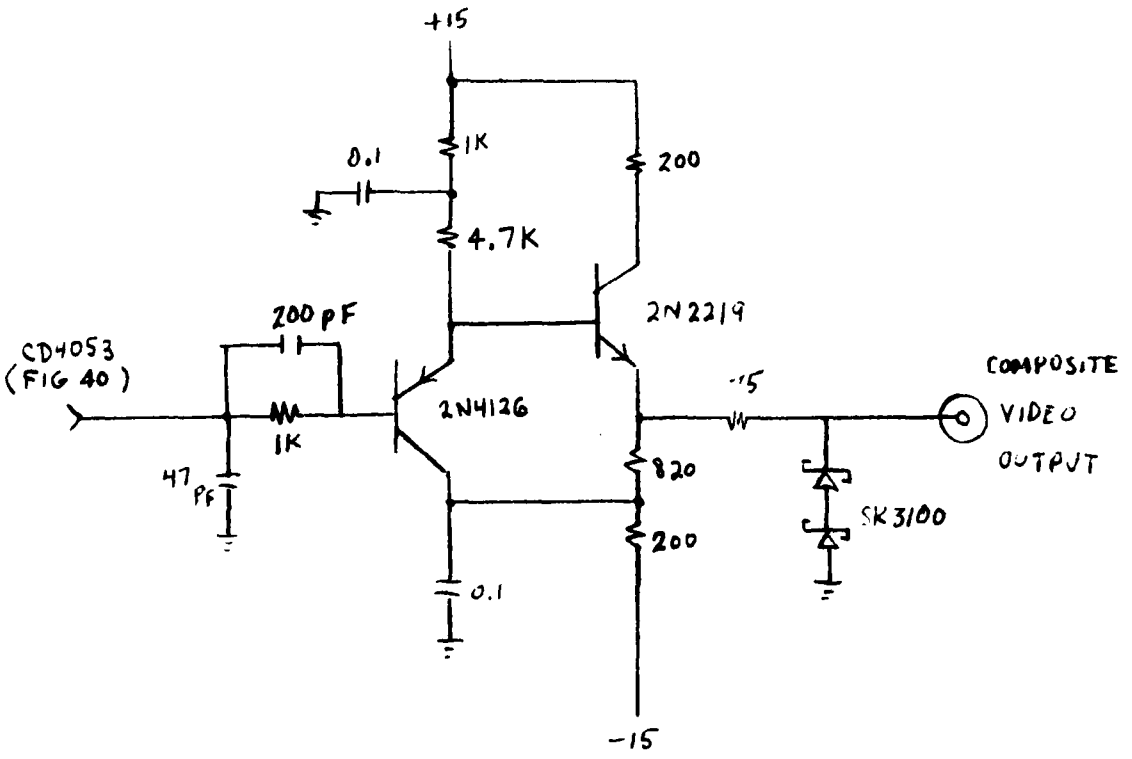


Figure 42 Video output amplifier

Power requirements were estimated on the basis of using low power schottky logic wherever possible. This approach was based upon the then current inavailability of high speed CMOS logic. The following voltages and currents were estimated for a special single power transformer: ± 24 V /1A, ± 15 V /1A, + 5 V /10A, - 5 V/1A and 40 V/0.1A. Bids were sought for this special transformer with output voltages somewhat higher to allow for dc regulators. A satisfactory transformer was fabricated by New England Transformer Co.

Two regulated multi-output supplies using these transformers were fabricated up to the point of wiring and mounting provisions being made in the SPU package. At this point a special Power Cube switching supply became available for trial use. At about the same time high speed CMOS logic circuits suddenly became available from a number of suppliers.

HCMOS and low power schottky logic circuits of the same type are pin for pin compatible. Thus, it was no major changeover to switch devices wherever possible. It was also decided to try the switching power supply. If the noise should turn out to be a problem there was always room to install the now overpowered linear supply. No noise problems were encountered that could be linked to the switching supply.

The circuitry in the Sensor head and the SPU take approximately 800 ma, or approximately 80 watts total power for all supplies.

C. Related Investigations

1. 64/128 gated clock

In the early days of this program the necessity arose for a gated output of either 64 or 128 pulses in a 40 μs interval between successive line drive pulses. The circuitry for this purpose is shown in Figure 43.

This circuit is similar to the GROCK - see Figures 14 and 15. The PLL operates at 12.915 MHz with an HC390 counter in the feedback path. The 12.915 MHz CK input to counter $HC163_1$ is divided down to obtain 1.6 MHz and 3.22 MHz at Q_C and Q_B respectively. These inputs to the mux HC157 are selected by the switch SW_1 for the CK input to the 120.

The remainder of the circuitry works in the same manner as the GROCK in

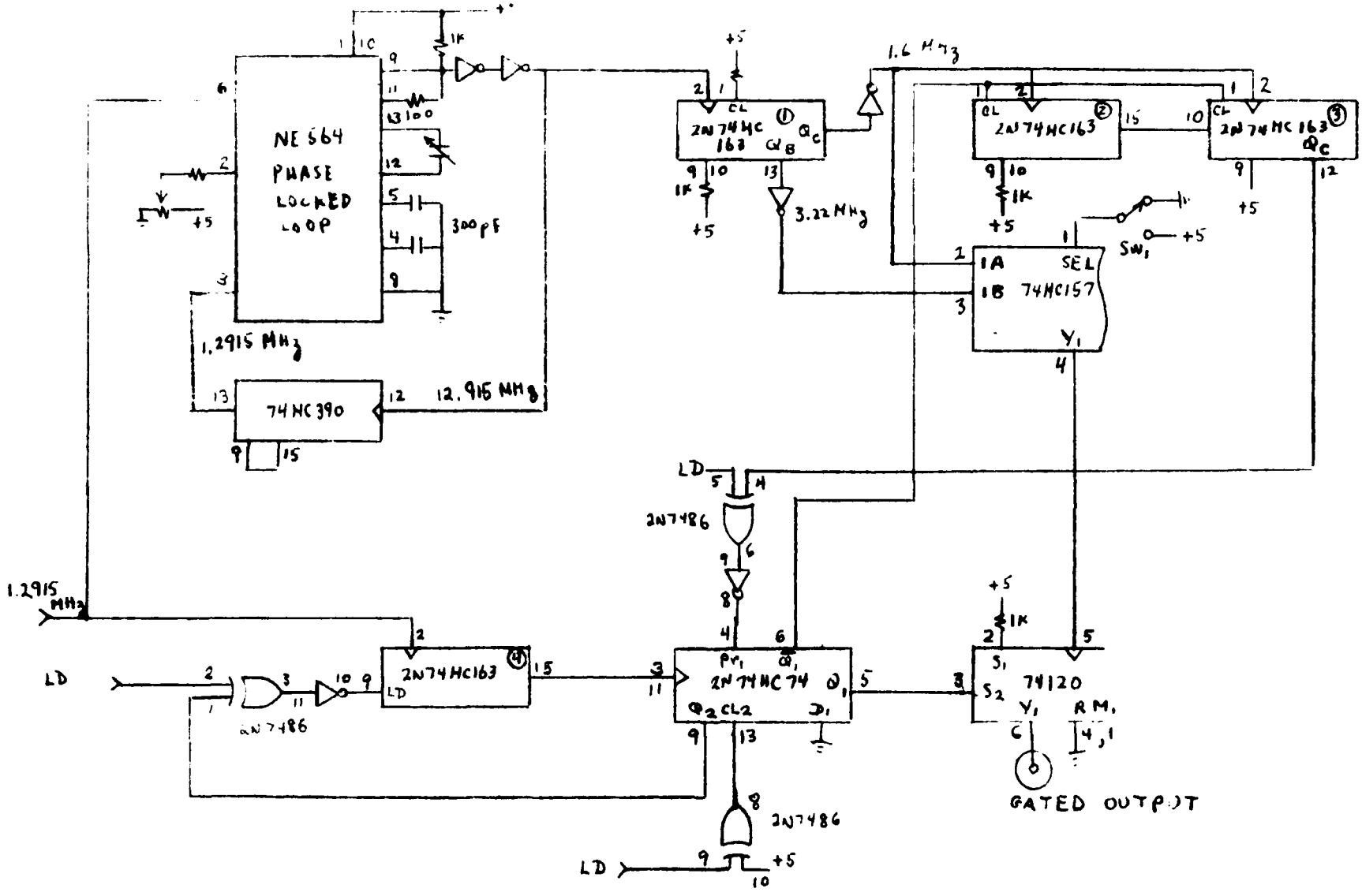


Figure 43 64/128 gated clock circuitry

producing a 40 μs wide gate pulse, to S_2 of the 120, which is located approximately symmetrically between LD pulses. The 40 μs interval is obtained using the 1.6 MHz for the CK input to counters $HC163_2$ and $HC163_3$.

Initially, at the onset of LD, Q_1 and $\overline{Q_1}$ are high and low respectively. The CK input to the "D" FF will drive Q_1 low and $\overline{Q_1}$ high since D_1 is always low. This initiates the pulse train operation at the output of the 120. 40 μs later the rising edge of Q_C of the counter $HC163_3$ will terminate the pulse train when Q_1 and S_2 go high and $\overline{Q_1}$ clears the counters.

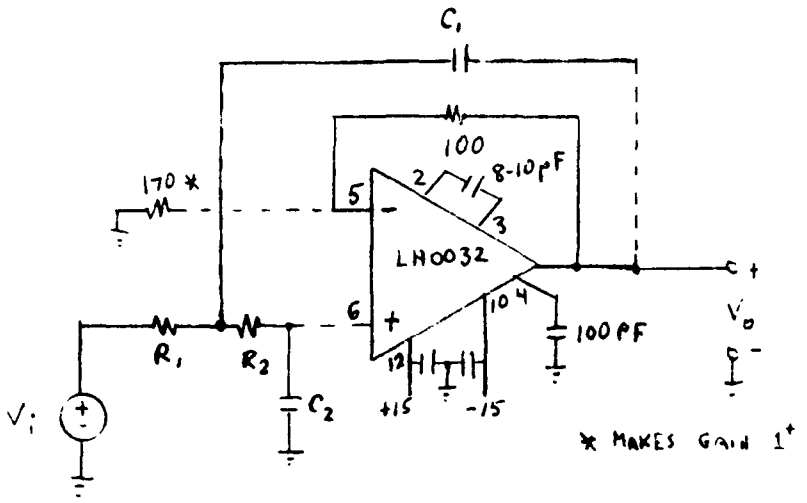
This circuit was found to function as predicted. Consequently a variation of it was used in designing the GROCK.

2. Active two pole filter

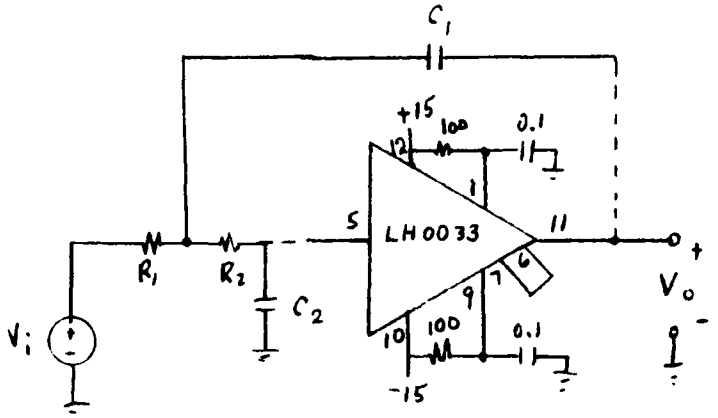
Considerable attention was given to the design and fabrication of an active low pass two pole filter. Since the upper half power point has been designated as 5 MHz the fabrication required care in the layout in order to minimize stray capacitance and inuctance. To this end PC boards were fabricated in house with ground planes and chip resistors and capacitors were used for each configuration.

Various operational amplifiers were tried in the Sallen-Key configuration. Some of these are shown in Figure 44. In Figure 44A the 170 ohms connected between Pin 5 and ground was used to adjust the gain slightly greater than unity. This will decrease the S coefficient of the denominator of the transfer function and thereby make it possible to more accurately tune the filter to the desired response.

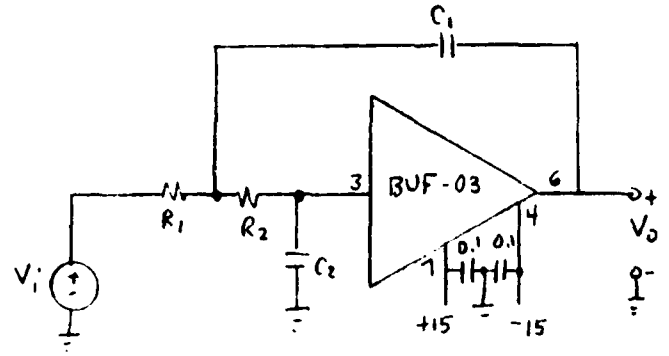
This particular configuration was investigated because of its simplicity and unity gain requirements. The OA's that showed the greatest promise were the LH0032, LH0033, and the BUF-03. A major drawback for the LH0032 was the number of components required for stable unity gain operation. The LH0033 proved more satisfactory, however, the calculated values of C_1 and C_2 needed to be halved to achieve the desired bandwidth. This was a reflection of the sensitivity of this device to stray capacity unaccounted for in the original design and the departure from unity gain. The BUF-03 was finally chosen on the basis of simplicity. This design was dicussed in Section 810.



(A)



(B)



(C)

Figure 44 Two pole Sallen-Key active filters

3. Switched gain amplifier

Many operational amplifiers have the characteristics that the gain-bandwidth product is a constant. That is, as the gain is increased the bandwidth is reduced proportionally. This is true for the PRAM used in the 64x128 camera for the switched gain amplifier. This is not a problem if the bandwidth for a gain of 8, the largest gain to be switched, is satisfactory. However, measurements on the PRAM indicated it would not be satisfactory for a bandwidth of 5 MHz.

The Comlinear CLC220 amplifier was specified as having a constant bandwidth for changes in gain. This was verified in the laboratory where the bandwidth was constant beyond 40 MHz for gains of magnitude between 1 and 10. The circuit used for this purpose is shown in Figure 45 for the inverting mode of operation. The same results were obtained for the noninverting mode.

The D/A board is direct coupled throughout. Consequently, a change in gain should not be accompanied by a dc level change other than that attributable to the desired analog signal. With nonideal OA's this is not possible. For the CLC 220 the variation in output level as the magnitude of the gain changed from 1 to 8 was significantly less in the inverting mode than in the noninverting mode. For this reason the final design of the switched gain amplifier is as shown in Figures 37 and 39.

4. Cryogenic cooler power source

Liquid nitrogen is used to cool the focal plane. The possibility of using a cryogenic cooler is an attractive alternative. One such cooler required 50 watts of power at an operating frequency of 50 Hz. The circuit designed and fabricated for this purpose is shown in Figure 46.

The ICL 8038, a function generator chip, is used to obtain the low voltage 50 Hz. It is inputted to a differential amplifier made up of two SK3528 low power PNP transistors. The output of the first differential stage is double ended to a second differential stage which serves as the driver stage for the output power transistors. The output complementary transistors used as the final stage are 2SK133 and 2SJ48 each with a collector dissipation of 100 watts. The supply voltage for these are $\pm$ 45

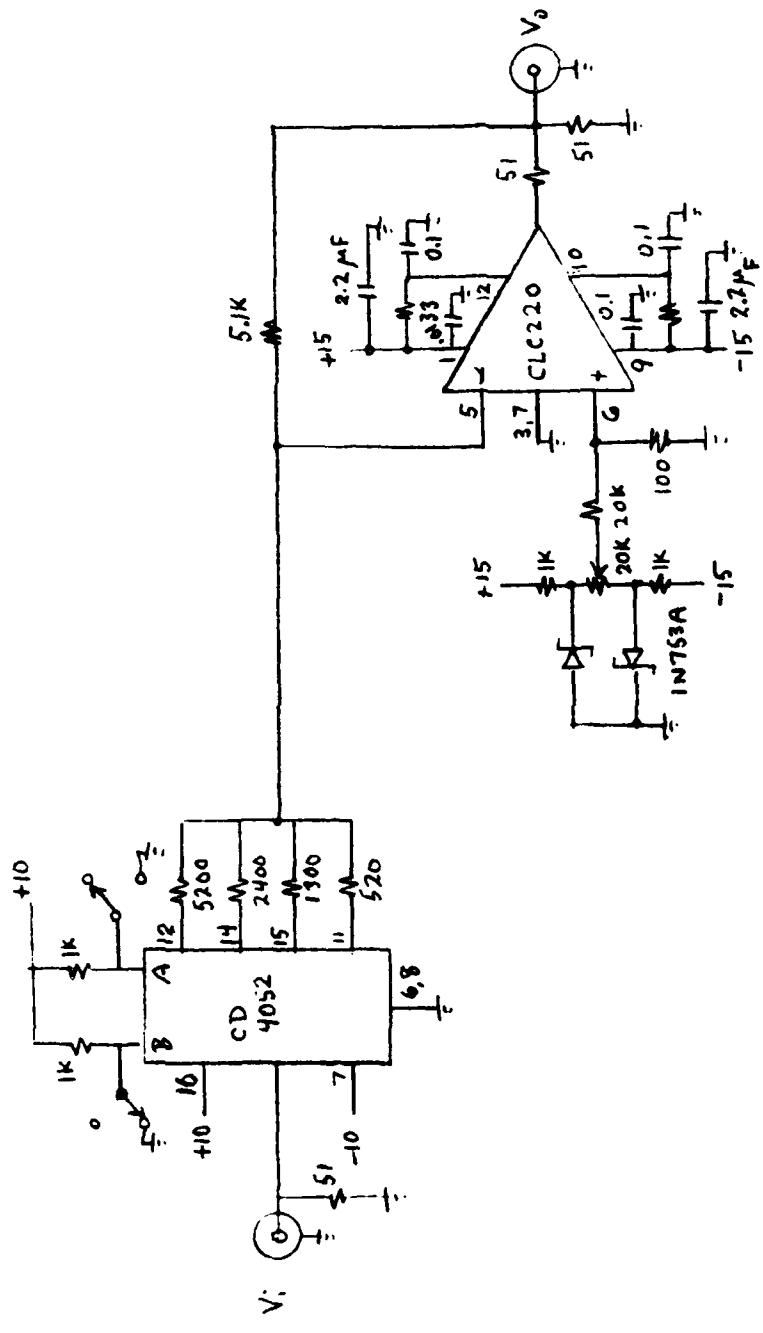


Figure 45 Switched gain amplifier circuit

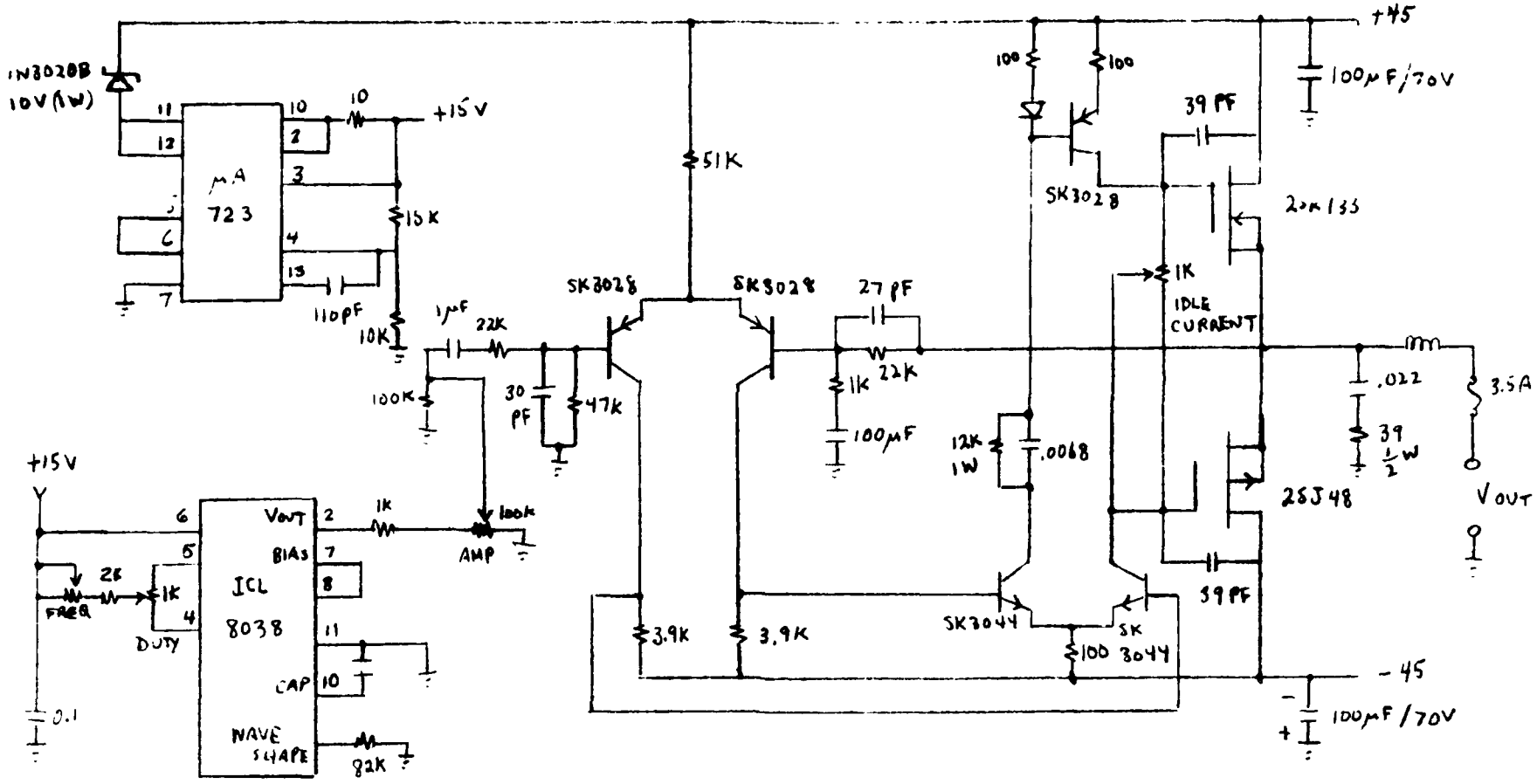


Figure 46 Cryogenic cooler power source

volts obtained from two commercial linear supplies with an output capability of three amperes. The low voltage required for the ICI 8038 is obtained from the -45 volt supply using a μA723 regulator with its output set for +15 volts. The output transistors were heat sinked and a small ac fan was used to help cool the entire 50 Hz power package.

The cryogenic cooler using this power source was used to cool the 256 element linear array. The power source ran surprisingly cool and has given no difficulty even after extended periods of operation.

SECTION III

CAMERA OPERATION AND APPLICATIONS

The 160x244 focal point is sensitive between 1 and 6 micrometers wavelength. The camera was operated with f/2 optics and a 3.5 micrometer long pass filter to suppress near visible, or reflected solar content in the imagery. Video displays were photographed for this report using the "FREEZE FRAME" capability of the camera.

The focal plane used to obtain these photographs was surprisingly free of defects as can be seen in Figure 46. For this reason it was really unnecessary to use the pixel correction procedures.

In evaluating the camera performance photographs were taken of television images with both z-axis (brightness) modulation and isometric modulation. With isometric modulation the video signal is added to the vertical component of the scanning raster at each pixel. The resulting "Isometric" display provides a relief map of the image where small signal variations are easily observed.

Figure 47a shows the uncompensated camera response to unfocussed background radiation at 25°C using z-axis modulation. The circular pattern is a map of doping variation in the silicon crystal. The faint plaid pattern is caused by lithographic errors. The bright spots show diodes with excess dark current. The dark spots, with the exception of the spot at the bottom center of the picture, are probably caused by dust on the backside of the focal plane. The dark spot at the bottom center of the picture is an inactive diode.

Figure 47b show the success of the 16-frame offset compensation. Sensitivity is now limited by infrared background noise, (background limited). Figure 48 shows the normal and compensated isometric images for unfocussed background radiation at 25°C.

Figure 49 is another example of the 16-frame offset compensation. In Figure 49a the camera signature seen in Figure 47a appears superimposed on the woman's face. After compensation, the image is free of these artifacts as indicated in Figure 49b.

The camera has a dynamic range in excess of 60 db and an MRT of less than 0.1°C which allows imaging measurements in scenes having substantial

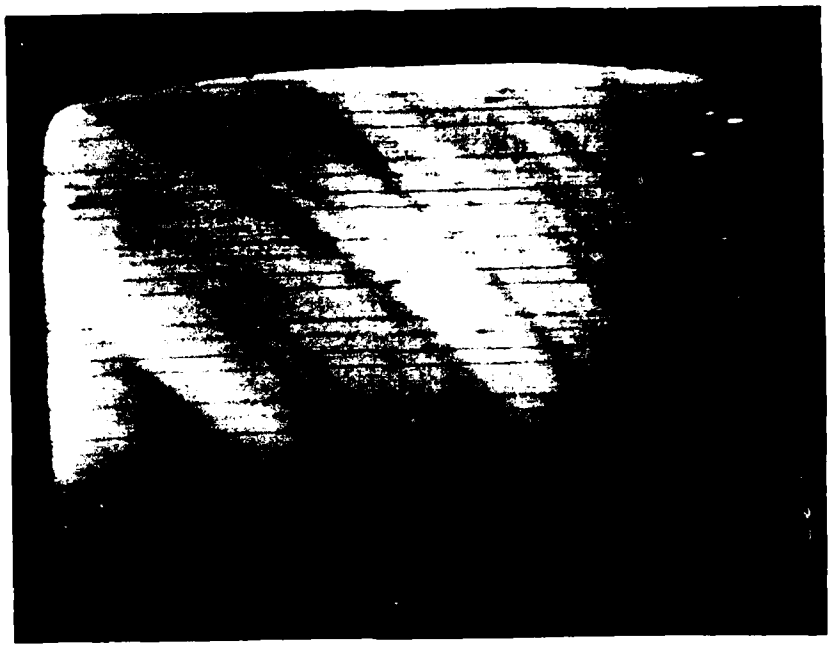


Figure 47a

Figure 47b

Figure 47. Unfocussed background response at 25°C
(a) uncompensated z-modulation
(b) compensated z-modulation

Figure 48a

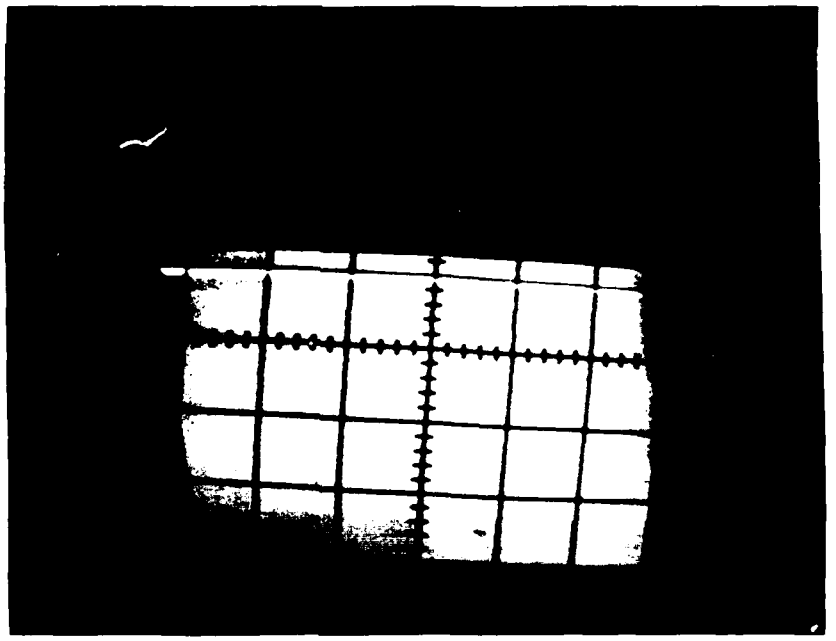


Figure 48b

Figure 48. Unfocussed background response at 25°C
(a) uncompensated isometric
(b) compensated isometric

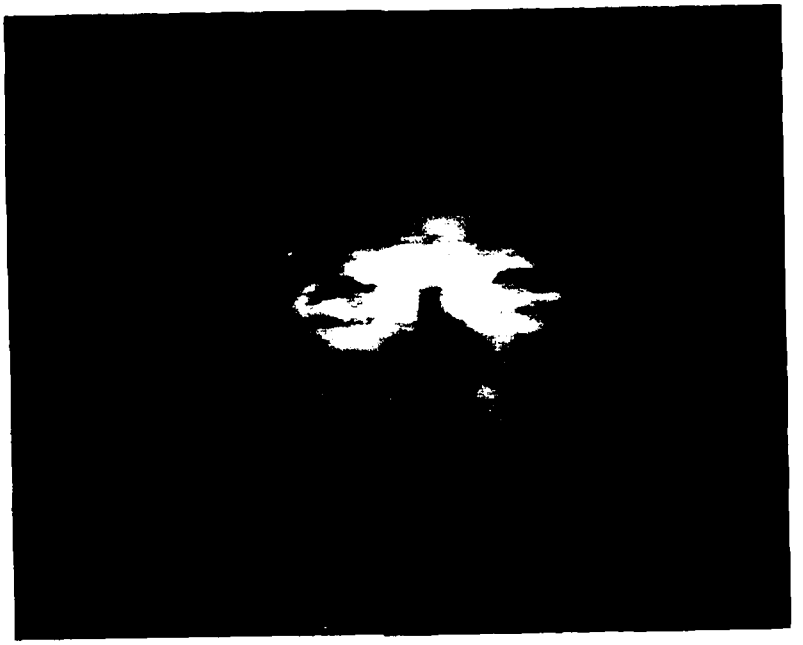


Figure 49a

Figure 49b

Figure 49.Woman's face
(a) uncompensated
(b) compensated

variations in brightness. This possibility is illustrated in Figure 50 where small changes in skin brightness, related to local variations in the man's vascular system, are clearly observable in the same frame as the hot pipe bowl. As another example note the detail in the womans profile in Figure 51. Her ear, the darkest (coolest) feature, reflects the limited blood flow in the cartilage of her ear.

Resolution of the 160x244 camera is improved over that of the 64x128 camera. This can be seen in Figure 52. Figure 52a is a photograph of a man and his pipe obtained from the smaller camera. Figure 52b is a similar picture obtained from the 160x244 camera. The black level setting is not quite the same, nor is the size the same, however the increased clarity of Figure 52b is apparent. Note the detail of the pipe stem in the two figures. In Figure 52a the stair case edges of the pipe stem are very evident reflecting the smaller number of pixels. In Figure 52b the stair case effect is significantly less. This same effect can be seen for the lefthand vertical edge of the glasses. Other evidence of improved resolution are in the details of the nose and mouth areas.

In the early evaluation of the camera reading glasses always appeared opaque, as in Figure 52. It was assumed the radiation from the eye area was blocked by the glasses. This assumption turned out to be false as indicated in Figure 53. Clearly the lefthand edge of the face of the subject is visible through the lefthand lens. This effect is not a function of the material of the glasses, plastic or glass, but rather the nature of the background of the subject being imaged. A high contrast temperature differential has to be here in order to see the transmission through the glasses.

Aside from the obious military applications the use of silicide sensors for medical measurements warrants serious considerations. In Figure 54 is shown the arterial map of the forearm of a young man who exercises regularly. Someone in poor health would show significantly weaker signals. Figure 55 shows the hand of a smoker in front of the hand of a nonsmoker. The smoker's skin temperature is cooler indicating reduced capillary performance near the surface of the skin.

The use of silicide camera technology for industrial applications could be extensive. The location and extent of chemical reactions in closed vessels could be determine from surface temperature mapping. An important

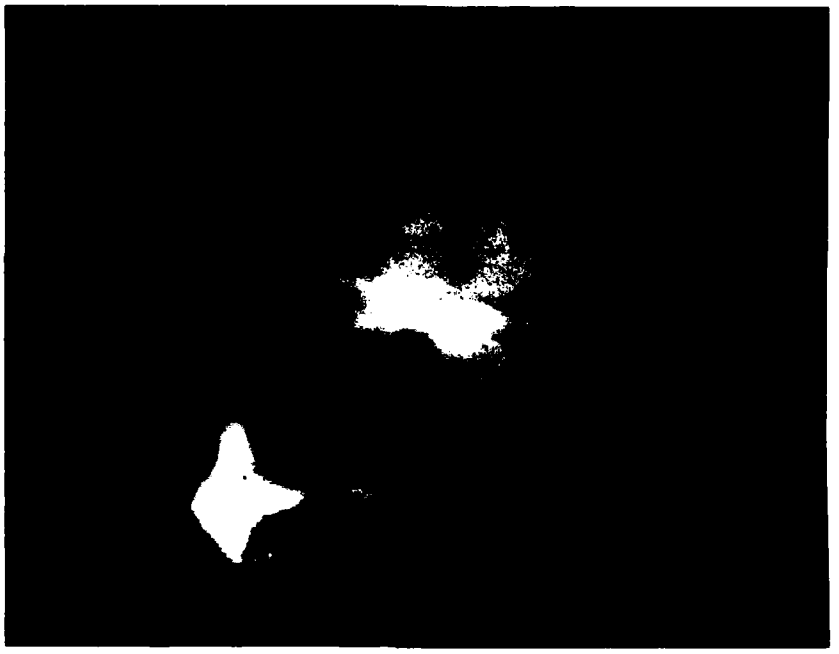


Figure 50. Wide dynamic range image showing both local skin temperature variations and hot pipe bowl

Figure 51. Woman's profile showing wide range of detail

Figure 52a

Figure 52b

Figure 52. Comparison of resolution
(a)64x128 camera
(b)160x244 camera

Figure 53. Thermal radiation through reading glasses

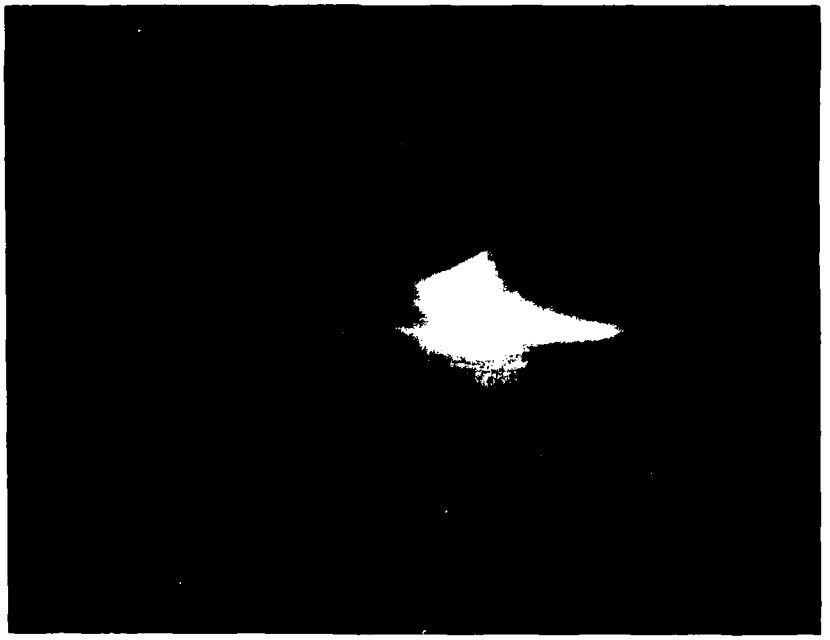


Figure 54. Vascular mapping of forearm

Figure 55. Comparison of surface temperature of smoker and nonsmoker

application would be the assessment of excessive power dissipation in electronic circuits or printed circuit board reliability. For example, Figure 56a shows the surface temperature of a PC board. Figure 56b shows the isometric display of the same image which could be calibrated for quantitative evaluation of the distribution of power dissipation.

Obviously numerous other applications are feasible. The point to be made is that this type of assessment is noninvasive, fast and easily documented by photograph.

Figure 56a

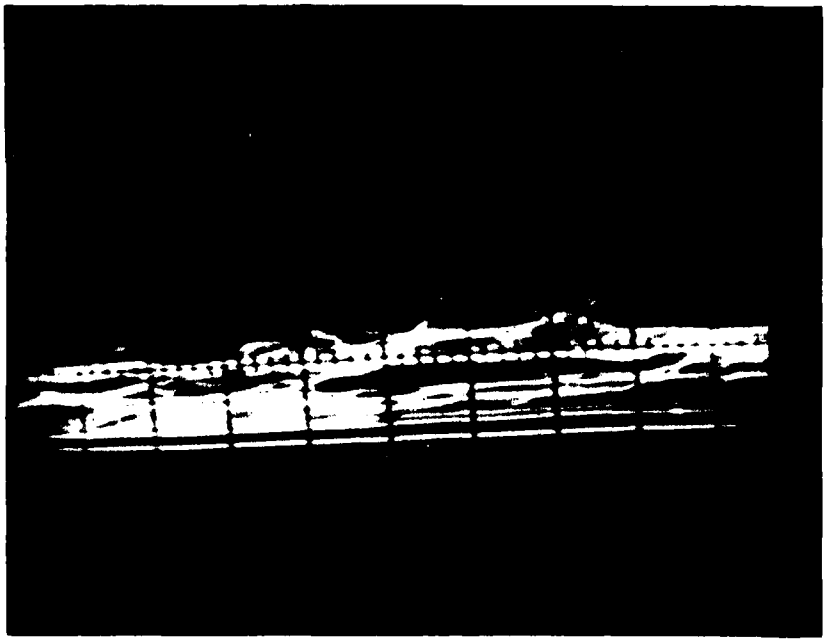


Figure 56b

Figure 56. Thermal map of operating PC board
(a) z-modulation
(b) isometric

SECTION IV

CONCLUSIONS

Successful operation of the 160x244 IRCCD camera has been demonstrated. However, improvements could be made in a second generation system. Some of these are related to design and others to fabrication.

The one-point correction, the 16 frame background averaging compensation, yields a significant improvement as noted in Figure 47b. Further improvement in the nonuniform responsivity of the detectors could be achieved by means of a two-point correction. Dynamic field balance correction (DFBC) could also lead to increased sensitivity at low signal levels.

From the viewpoint of fabrication, different plugin cards should be used. These should have ground planes and not require wire wrapping for the memory cards. The plugin boards should in some cases be partitioned more carefully. This observation arose in the debugging procedure where it was found necessary to reroute certain connections to prevent spurious interaction of control signals.

The use of larger memories, say 32Kx16 bit chips, should be considered. These may lead to addressing simplification and obviously shrink the size of the SPU by using fewer boards. Of course this possible reduction in size coud be partially negated by the suggested improvements in design which would require additional space.

In summary, silicide IRCCD cameras have advanced in performance to where they are candidates for wide ranging industrial, medical and scientific applications. This report has presented examples of imagery which show the performance of the 160x244 IRCCD camera and which indicate the near term potential for applications of this technology.

SECTION V

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SECTION VI

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To Kenneth Vaccaro, an undergraduate student, who enthusiastically contributed to the fabrication and evaluation of the original design.

SECTION VII

PUBLICATIONS

A paper based on this work was presented on 29 November 1985 at the 2nd International Technical Symposium on Optical and Electro-Optical Applied Sciences and Engineering. The title and abstract follow below:

Platinum Silicide Sensor Imagery

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ABSTRACT

Infrared television cameras, based upon platinum silicide photodiode arrays, have advanced in sensitivity, resolution and reliability to where they could have wide ranging application to medical, industrial and scientific measurement. In this paper we will present examples of silicide camera imagery which show the sort of data which might be expected from such measurements.

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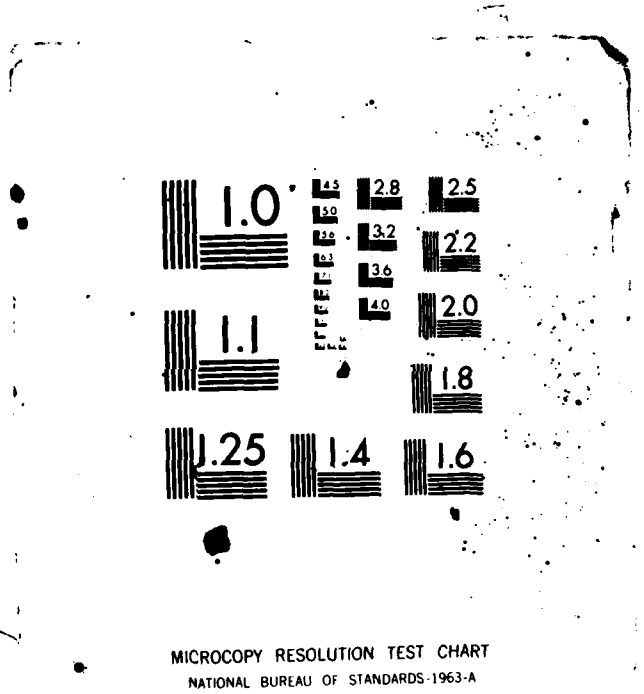
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